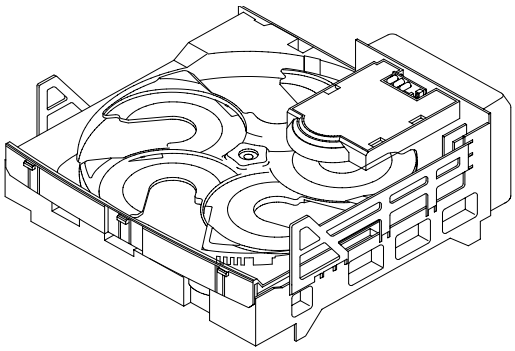
aiwa SERVICE

6ZG-1

English



SERVICE MANUAL

CD MECHANISM

BASIC CD MECHANISM : 3ZG-2 E1

TYPE
YSDFNSHCM
VOS1NDSM
YVOS1NDM
YSDNSHM
SDFNSHM

aiwa

S/M Code No. 09-994-326-2N2

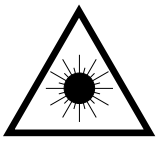
TABLE OF CONTENTS

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!

WHEN SERVICING, DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION. BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICK-UP BLOCK.



- Caution: Invisible laser radiation when open and interlocks defeated avoid exposure to beam.
- Advarsel: Usynling laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

VAROITUS!

Laiteen Käyttäminen muulla kuin tässä käyttöohjeessa mainitulla tavalla saattaa altistaa käyt-täjän turvallisuusluokan 1 ylittävälle näkymättömälle lasersäteilylle.

VARNING!

Om apparaten används på annat sätt än vad som specificeras i denna bruksanvising, kan användaren utsättas för osynling laserstrålning, som överskrider gränsen för laserklass 1.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

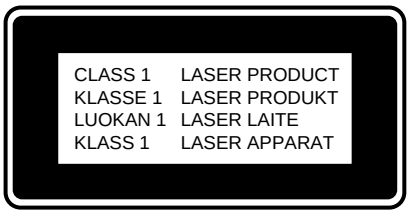
ATTENTION

L'utilisation de commandes, réglages ou procédures autres que ceux spécifiés peut entraîner une dangereuse exposition aux radiations.

ADVARSEL!

Usynlig laserstråling ved åbning, når sikkerhedsafbrydereer ude af funktion. Undgå udsættelse for stråling.

This Compact Disc player is classified as a CLASS 1 LASER product.
The CLASS 1 LASER PRODUCT label is located on the rear exterior.

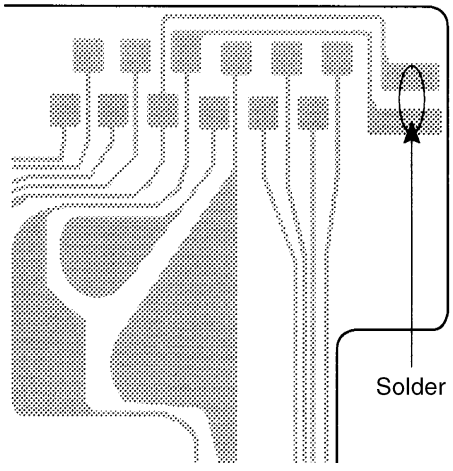


Precaution to replace Optical block (KSS-213B)

Body or clothes electrostatic potential could ruin laser diode in the optical block. Be sure ground body and workbench, and use care the clothes do not touch the diode.

1) After the connection, remove solder shown in the right figure.

PICK-UP Assy P.C.B



DISASSEMBLY INSTRUCTIONS

1. How to replace PICK UP.

1) Open the TRAY.
   Push the stopper to arrow direction and release half of the SHAFT SLED.
2) Turn GEAR MAIN CAM to the counterclockwise (arrow “a”) direction, and lift up CD mechanism. (Fig-1)
3) Remove SHAFT SLED.
4) CD mechanism in down position, replace PICK UP.
5) Lift up CD mechanism (Fig-1), and Reassemble the SHAFT SLED.

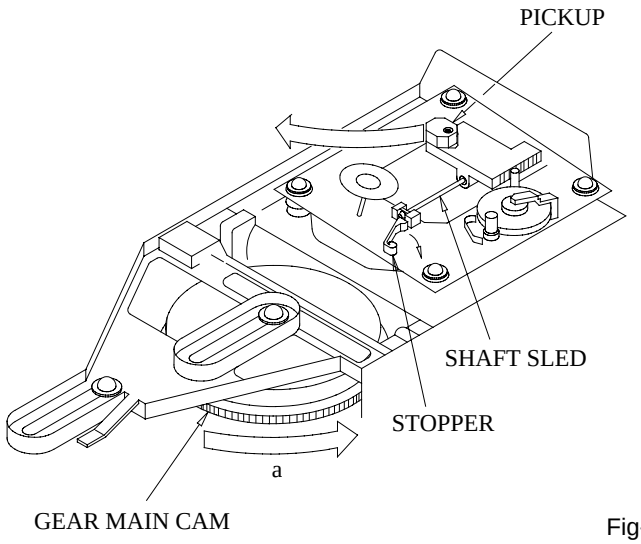


Fig-1

2. How to remove the 5CD CHANGER BLOCK (Fig-2)

1) Remove the two FFC of the CD circuit board, and remove the five SCREWS.
2) Lift 5 CD CHANGER BLOCK from behind, and remove it. (5CD CHANGER BLOCK can be removed even if PANEL TRAY is not removed.)

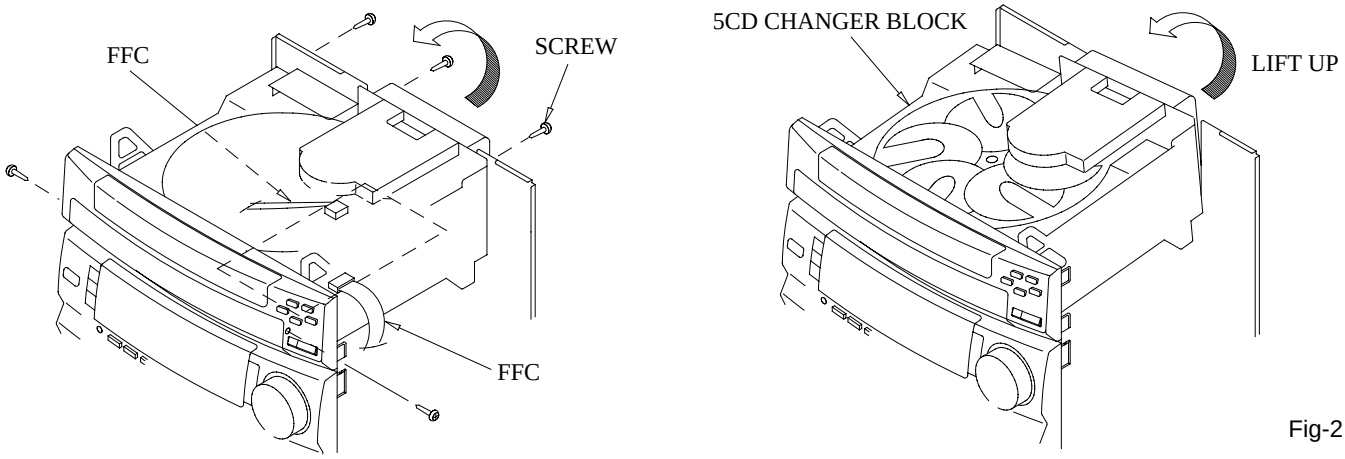


Fig-2

3. The disassemble and reassemble the TRAY

3-1. Disassembling procedure.

1) Push the PLATE GEAR'S Boss at the bottom part of CHAS MECHA strongly to the outside (arrow "b" direction). (Fig-3)
   (Confirm that TRAY appears a little in the front.)
2) Draw TRAY to the open position.
3) Remove FFC, and push the two LEVERS at both side of the CHAS MECH to remove TRAY. (Fig-4)

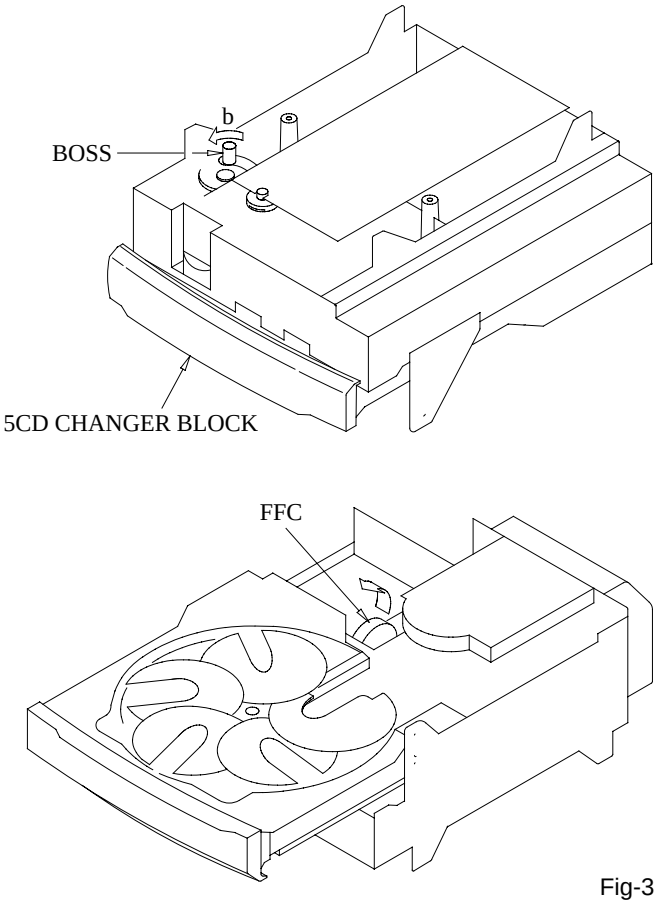


Fig-3

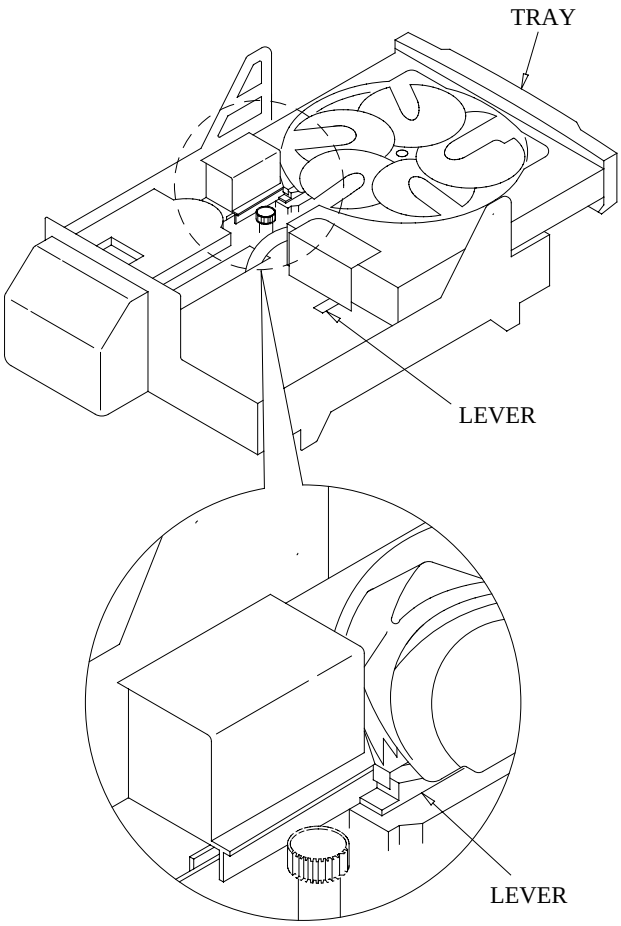


Fig-4

3-2. Reassembling procedure.

1) Confirm that LEVER TRAY is at the most right position and check for the CD Mechanism to be in the down position. (Fig-5)
2) Push in the TRAY along the rail of the CHAS MECHA.
3) After TRAY is half closed and FFC is put in, it can enter by force until the end of TRAY closed. (Fig-6)

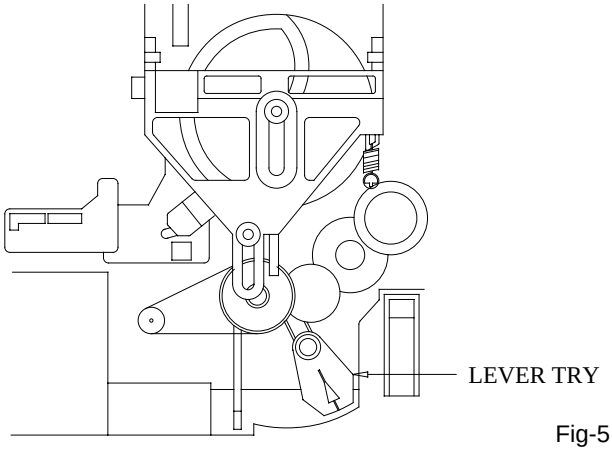


Fig-5

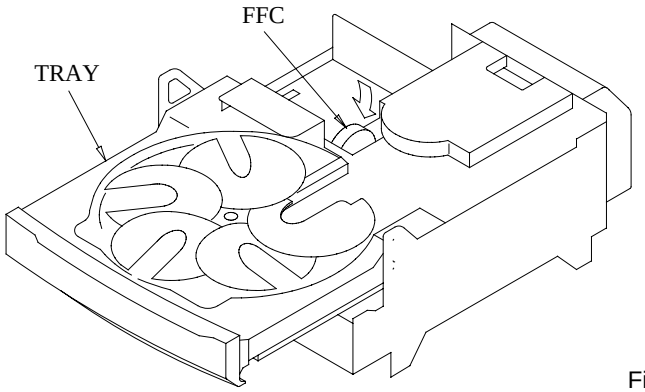


Fig-6

4. How to reassemble the TURN TABLE. (Fig-7)

1) Push LEVER TT in the direction of “C”, and put in the TURN TABLE 5CD. (Fig-7)
After reassembly, one of the TURN TABLE DISC TRAY (can be either one of the five disc trays) must be aligned with TURN TABLE 5CD. (Fig-8)
That is, having no gap difference between the TURN TABLE 5CD and the TRAY 5CD.

* When reassembling the TURN TABLE 5CD, it is acceptable facing any CD number (1-5).

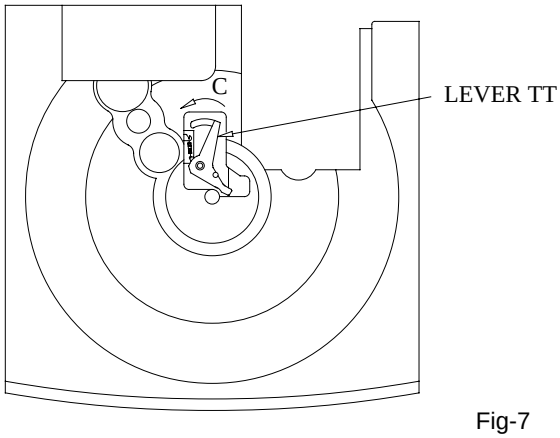


Fig-7

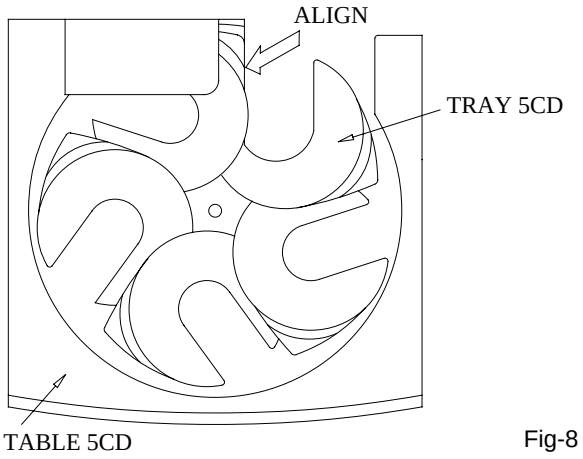


Fig-8

ELECTRICAL MAIN PARTS LIST

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
IC			
	87-A20-547-010		C-IC,CXA1992AR<EXCEPT YSDFNSHCM>
	87-A20-919-040		C-IC,BA5915FP<YVOS1NDM,VOS1NDSM>
	87-A20-917-010		C-IC,CXD2540Q-1/2 <YVOS1NDM,VOS1NDSM>
	87-A20-546-010		C-IC,CXD2589Q<SDFNSHM,YSDNSHM>
	87-A20-592-040		C-IC,M51943 AML<EXCEPT YSDFNSHCM>
	87-A20-602-040		C-IC,M5291FP<YVOS1NDM,VOS1NDSM>
	87-A20-925-040		C-IC,BA05FP<YVOS1NDM,VOS1NDSM>
	87-A20-905-040		C-IC,BA033FP<YVOS1NDM,VOS1NDSM>
	87-070-305-010		IC,BA6897S<SDFNSHM,YSDNSHM>
	87-001-982-010		IC,TA7291S<EXCEPT YSDFNSHCM>
	87-A20-918-040		C-IC,SM5878AM<YVOS1NDM,VOS1NDSM>
	87-A20-653-010		C-IC,RL5C293<YVOS1NDM,VOS1NDSM>
	87-017-825-010		IC,GP1F32T<YVOS1NDM,VOS1NDSM>
	86-ZG1-658-010		C-IC,CXP84548-112Q <YVOS1NDM,VOS1NDSM>
	87-A20-895-010		C-IC,CXD1856R<YVOS1NDM,VOS1NDSM>
	87-A20-921-040		C-IC,SN74LVU04APW <YVOS1NDM,VOS1NDSM>
	87-A20-249-040		C-IC,BU2874FV<YVOS1NDM,VOS1NDSM>
	87-A20-962-040		C-IC,MSM54V16258B/BSL <YVOS1NDM,VOS1NDSM>
	87-A20-957-040		C-IC,SN74LV245APW <YVOS1NDM,VOS1NDSM>
	86-ZG1-655-040		C-IC,MSM531031B-72GS-KR1 <YVOS1NDM,VOS1NDSM>
	87-A21-099-040		C-IC,HD74HC393FP <YVOS1NDM,VOS1NDSM>
TRANSISTOR			
	89-406-555-080		TR,2SD655 (0.5W)<SDFNSHM,YSDNSHM>
	89-111-625-080		TR,2SA1162 (0.15W) <YVOS1NDM,VOS1NDSM>
	87-026-463-080		TR,2SA933S (0.3W) <SDFNSHM,YSDNSHM>
	87-026-237-080		CHIP-TR,DTC124XK <YVOS1NDM,VOS1NDSM>
	87-A30-117-010		TR,2SA1357<YVOS1NDM,VOS1NDSM>
	87-026-231-080		CHIP-TRANSISTER,DTA124XK <YVOS1NDM,VOS1NDSM>
	89-421-722-380		TR,2SD2172V/W<EXCEPT YSDFNSHCM>
	89-320-011-080		TR,2SC2001 (15W) <EXCEPT YSDFNSHCM>
	87-026-223-080		TR,DTC143TK<EXCEPT YSDFNSHCM>
	89-110-155-080		TR,2SA1015(0.4W)<SDFNSHM,YSDNSHM>
	87-026-580-080		C-TR,DTA123JK<EXCEPT YSDFNSHCM>
	89-327-125-080		CHIP TR,2SC2712GR <EXCEPT YSDFNSHCM>
	87-026-470-080		TR,HN1C03F (0.3W) <YVOS1NDM,VOS1NDSM>
	87-026-210-080		CHIP-TR,DTC144EK <YVOS1NDM,VOS1NDSM>
DIODE			
	87-020-027-080		CHIP-DIODE 1SS184 <YVOS1NDM,VOS1NDSM>
	87-020-465-080		DIODE,1SS133 (110MA) <SDFNSHM,YSDNSHM>
	87-A40-180-040		C-DIODE,SB07-015C <YVOS1NDM,VOS1NDSM>
	87-018-199-080		CAP, CER 3300P<SDFNSHM,YSDNSHM>
5CD C.B<EXCEPT YVOS1NDM,V 1NDSM>			
	86-ZG1-605-010		CABLE,FFC 16P
	86-ZG1-667-010		F-CABLE,8P 1.25 175MM BLACK
C1	87-010-196-080		CHIP CAPACITOR,0.1-25
C2	87-010-260-080		CAP, ELECT 47-25V
C4	87-010-197-080		CAP, CHIP 0.01 DM
C101	87-010-263-040		CAP,E 100-10
C102	87-010-178-080		CHIP CAP 1000P
C103	87-010-550-040		CAP,E 100-6.3 GAS
C104	87-010-182-080		C-CAP,S 2200P-50 B
C105	87-010-198-080		CAP, CHIP 0.022
C106	87-016-081-080		C-CAP,S 0.1-16 RK
C107	87-016-081-080		C-CAP,S 0.1-16 RK
C108	87-016-081-080		C-CAP,S 0.1-16 RK
C109	87-010-497-040		CAP,E 4.7-35 GAS
C110	87-016-081-080		C-CAP,S 0.1-16 RK
C111	87-010-197-080		CAP, CHIP 0.01 DM
C112	87-010-402-040		CAP,E 2.2-50
C113	87-010-382-040		CAP,E 22-25 SME
C114	87-010-213-080		C-CAP,S 0.015-50 B
C115	87-010-263-040		CAP,E 100-10
C116	87-010-197-080		CAP, CHIP 0.01 DM
C117	87-010-369-080		C-CAP,S 0.033-25 K B
C118	87-010-197-080		CAP, CHIP 0.01 DM
C119	87-010-369-080		C-CAP,S 0.033-25 K B
C120	87-010-197-080		CAP, CHIP 0.01 DM
C121	87-010-494-040		CAP,E 1-50 GAS
C122	87-010-154-080		CAP CHIP 10P
C123	87-010-154-080		CAP CHIP 10P
C124	87-010-154-080		CAP CHIP 10P
C125	87-010-596-080		CAP, S 0.047-16
C126	87-010-596-080		CAP, S 0.047-16
C127	87-012-140-080		CAP 470P
C128	87-010-596-080		CAP, S 0.047-16
C129	87-010-198-080		CAP, CHIP 0.022
C130	87-016-081-080		C-CAP,S 0.1-16 RK
C131	87-010-550-040		CAP,E 100-6.3 GAS
C132	87-010-550-040		CAP,E 100-6.3 GAS
C133	87-012-158-080		C-CAP,S 390P-50 CH
C150	87-010-145-080		C-CAP,S 1P-50 CH
C202	87-010-596-080		CAP, S 0.047-16
C203	87-010-188-080		CAP,CHIP 6800P
C204	87-012-156-080		C-CAP,S 220P-50 CH
C205	87-018-134-080		CAPACITOR,TC-U 0.01-16
C206	87-010-400-040		CAP,E 0.47-50
C207	87-010-197-080		CAP, CHIP 0.01 DM
C208	87-010-318-080		C-CAP,S 47P-50 CH
C209	87-012-154-080		C-CAP,S 150P-50 CH
C210	87-012-154-080		C-CAP,S 150P-50 CH
C211	87-010-176-080		C-CAP,S 680P-50 SL
C212	87-010-176-080		C-CAP,S 680P-50 SL
C213	87-010-401-040		CAP,E 1-50 SME
C213	87-010-382-040		CAP,E 22-25 SME
C214	87-010-401-040		CAP,E 1-50 SME
C214	87-010-382-040		CAP,E 22-25 SME
C215	87-010-318-080		C-CAP,S 47P-50 CH
C216	87-010-318-080		C-CAP,S 47P-50 CH
C217	87-010-380-040		CAP,E 47-16 SME
C218	87-010-197-080		CAP, CHIP 0.01 DM
C219	87-010-196-080		CHIP CAPACITOR,0.1-25
C220	87-010-370-040		CAP,E 330-6.3 SME
C221	87-010-197-080		CAP, CHIP 0.01 DM
C222	87-010-186-080		CAP,CHIP 4700P
C223	87-016-081-080		C-CAP,S 0.1-16 RK
C228	87-018-209-080		CAP, CER 0.1-50V
C230	87-010-197-080		CAP, CHIP 0.01 DM
C231	87-018-209-080		CAP, CER 0.1-50V
C401	87-010-403-080		CAP, ELECT 3.3-50V
C402	87-010-403-040		CAP,E 3.3-50 SME
C501	87-016-459-040		CAP,E 470-10 SMG
C502	87-010-197-080		CAP, CHIP 0.01 DM
C503	87-010-263-040		CAP,E 100-10
C504	87-010-196-080		CHIP CAPACITOR,0.1-25
C505	87-010-196-080		CHIP CAPACITOR,0.1-25
C506	87-010-196-080		CHIP CAPACITOR,0.1-25
C507	87-010-196-080		CHIP CAPACITOR,0.1-25

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
C508	87-016-459-040		CAP,E 470-10 SMG
C509	87-010-196-080		CHIP CAPACITOR,0.1-25
C510	87-010-196-080		CHIP CAPACITOR,0.1-25
C601	87-010-197-080		CAP, CHIP 0.01 DM
C602	87-016-251-040		CAP,E 220-16 SMG
C603	87-010-196-080		CHIP CAPACITOR,0.1-25
C701	87-010-322-080		C-CAP,S 100P-50 CH
C702	87-010-318-080		C-CAP,S 47P-50 CH
C703	87-010-318-080		C-CAP,S 47P-50 CH
C705	87-010-178-080		CHIP CAP 1000P
C901	87-010-260-040		CAP,E 47-25 SME
C902	87-010-196-080		CHIP CAPACITOR,0.1-25
C991	87-010-196-080		CHIP CAPACITOR,0.1-25
C992	87-010-196-080		CHIP CAPACITOR,0.1-25
C993	87-010-196-080		CHIP CAPACITOR,0.1-25
C994	87-010-196-080		CHIP CAPACITOR,0.1-25
CN3	86-ZG1-609-010		CONN ASSY,6P
CN7	86-ZG1-606-010		CONN ASSY 2P
CON1	87-A60-424-010		CONN,16P V TOC-B
CON2	87-009-034-010		CONN,6P PH V
CON3	87-A60-133-010		CONN,8P V FE
CON5	87-A60-154-010		CONN,6P H FE
CON6	87-A60-162-010		CONN,14P H FE
JR9	83-XM1-617-080		C-COIL,BK2125HM601
JR28	83-XM1-617-080		C-COIL,BK2125HM601
JW8	87-018-115-080		CAP, CER 47P-50V
JW42	87-003-223-010		FERRITE BEAD BLO2RN2
JW47	87-003-223-010		FERRITE BEAD BLO2RN2
JW48	87-026-689-080		PROTECTOR,1A 60V 491
JW72	87-003-223-010		FERRITE BEAD BLO2RN2
L101	87-003-102-080		COIL, 10UH
L201	87-003-102-080		COIL, 10UH
LED901	87-A40-123-010		LED,SLZ-8128A-01-B
M601	87-045-305-010		MOTOR, RF-500TB DC-5V (2MA)
R101	87-022-363-080		C-RES,S 68K-1/10W F
R102	87-022-363-080		C-RES,S 68K-1/10W F
R103	87-022-363-080		C-RES,S 68K-1/10W F
R104	87-022-363-080		C-RES,S 68K-1/10W F
R105	87-022-365-080		C-RES,S 100K-1/10W F
R106	87-022-365-080		C-RES,S 100K-1/10W F
R420	87-029-060-080		RES,FUSE 33-1/4 W
SW601	87-036-109-010		PUSH SWITCH
SW602	87-036-109-010		PUSH SWITCH
SW603	87-036-109-010		PUSH SWITCH
X201	87-A70-046-010		VIB,XTAL 16.934MHZ

VCD C.B<YVOS1NDM,VOS1NDSM

	86-ZG1-605-010		CABLE,FFC 16P
	86-ZG1-667-010		F-CABLE,8P 1.25 175MM BLACK
C101	87-010-182-080		C-CAP,S 2200P-50 B
C102	87-016-669-080		C-CAP,S 0.1-25 K B
C103	87-016-669-080		C-CAP,S 0.1-25 K B
C104	87-016-669-080		C-CAP,S 0.1-25 K B
C105	87-010-404-040		CAP,E 4.7-50 SME
C106	87-010-369-080		C-CAP,S 0.033-25 K B
C107	87-010-197-080		CAP, CHIP 0.01 DM
C108	87-010-401-040		CAP,E 1-50 SME
C109	87-010-382-040		CAP,E 22-25 SME
C110	87-010-213-080		C-CAP,S 0.015-50 B
C111	87-010-263-040		CAP,E 100-10
C112	87-010-197-080		CAP, CHIP 0.01 DM
C113	87-010-369-080		C-CAP,S 0.033-25 K B
C114	87-010-369-080		C-CAP,S 0.033-25 K B
C115	87-010-369-080		C-CAP,S 0.033-25 K B
C116	87-012-158-080		C-CAP,S 390P-50 CH
C117	87-012-154-080		C-CAP,S 150P-50 CH
C118	87-010-401-040		CAP,E 1-50 SME
C119	87-010-311-080		CAP 12P
C120	87-010-596-080		CAP, S 0.047-16
C121	87-010-596-080		CAP, S 0.047-16
C123	87-016-669-080		C-CAP,S 0.1-25 K B
C125	87-010-198-080		CAP, CHIP 0.022
C126	87-016-669-080		C-CAP,S 0.1-25 K B
C127	87-010-263-040		CAP,E 100-10
C130	87-010-263-040		CAP,E 100-10
C131	87-010-263-040		CAP,E 100-10
C132	87-010-178-080		CHIP CAP 1000P
C133	87-010-263-040		CAP,E 100-10
C134	87-010-196-080		CHIP CAPACITOR,0.1-25
C135	87-010-196-080		CHIP CAPACITOR,0.1-25
C136	87-010-196-080		CHIP CAPACITOR,0.1-25
C137	87-010-196-080		CHIP CAPACITOR,0.1-25
C138	87-010-182-080		C-CAP,S 2200P-50 B
C139	87-010-197-080		CAP, CHIP 0.01 DM
C140	87-010-384-040		CAP,E 100-25 SME
C141	87-010-196-080		CHIP CAPACITOR,0.1-25
C142	87-010-196-080		CHIP CAPACITOR,0.1-25
C143	87-010-197-080		CAP, CHIP 0.01 DM
C144	87-010-196-080		CHIP CAPACITOR,0.1-25
C145	87-010-196-080		CHIP CAPACITOR,0.1-25
C149	87-010-213-080		C-CAP,S 0.015-50 B
C151	87-010-263-040		CAP,E 100-10
C152	87-010-197-080		CAP, CHIP 0.01 DM
C153	87-016-251-040		CAP,E 220-16 SMG
C154	87-010-196-080		CHIP CAPACITOR,0.1-25
C155	87-010-184-080		CHIP CAPACITOR 3300P(K)
C156	87-016-669-080		C-CAP,S 0.1-25 K B
C157	87-010-992-080		C-CAP,S 0.047-25 B
C158	87-012-156-080		C-CAP,S 220P-50 CH
C159	87-016-526-080		C-CAP,S 0.47-16 BK
C160	87-010-197-080		CAP, CHIP 0.01 DM
C161	87-010-182-080		C-CAP,S 2200P-50 B
C300	87-010-197-080		CAP, CHIP 0.01 DM
C301	87-016-251-040		CAP,E 220-16 SMG
C302	87-012-140-080		CAP 470P
C303	87-010-178-080		CHIP CAP 1000P
C304	87-010-384-040		CAP,E 100-25 SME
C305	87-010-384-040		CAP,E 100-25 SME
C306	87-016-251-040		CAP,E 220-16 SMG
C307	87-010-196-080		CHIP CAPACITOR,0.1-25
C308	87-010-263-040		CAP,E 100-10
C309	87-010-196-080		CHIP CAPACITOR,0.1-25
C310	87-010-263-040		CAP,E 100-10
C311	87-010-196-080		CHIP CAPACITOR,0.1-25
C312	87-010-178-080		CHIP CAP 1000P
C401	87-010-403-040		CAP,E 3.3-50 SME
C402	87-010-403-040		CAP,E 3.3-50 SME
C411	87-018-214-080		CAP TC U 0.1-50F
C601	87-010-197-080		CAP, CHIP 0.01 DM
C602	87-016-251-040		CAP,E 220-16 SMG
C603	87-010-196-080		CHIP CAPACITOR,0.1-25
C706	87-010-184-080		CHIP CAPACITOR 3300P(K)
C707	87-010-184-080		CHIP CAPACITOR 3300P(K)
C708	87-010-184-080		CHIP CAPACITOR 3300P(K)
C709	87-010-184-080		CHIP CAPACITOR 3300P(K)
C801	87-010-197-080		CAP, CHIP 0.01 DM
C802	87-010-197-080		CAP, CHIP 0.01 DM
C803	87-010-384-040		CAP,E 100-25 SME
C804	87-010-196-080		CHIP CAPACITOR,0.1-25
C805	87-010-196-080		CHIP CAPACITOR,0.1-25
C806	87-010-196-080		CHIP CAPACITOR,0.1-25
C807	87-010-313-080		CAP, CHIP 18P
C808	87-010-313-080		CAP, CHIP 18P
C809	87-010-178-080		CHIP CAP 1000P
C810	87-010-178-080		CHIP CAP 1000P
C811	87-010-178-080		CHIP CAP 1000P
C812	87-010-178-080		CHIP CAP 1000P
C813	87-010-405-040		CAP,E 10-50
C814	87-010-405-040		CAP,E 10-50

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
C815	87-010-318-080		C-CAP,S 47P-50 CH
C816	87-010-318-080		C-CAP,S 47P-50 CH
C851	87-010-197-080		CAP, CHIP 0.01 DM
C852	87-010-197-080		CAP, CHIP 0.01 DM
C853	87-010-196-080		CHIP CAPACITOR,0.1-25
C854	87-010-196-080		CHIP CAPACITOR,0.1-25
C855	87-010-197-080		CAP, CHIP 0.01 DM
C856	87-012-140-080		CAP 470P
C857	87-012-140-080		CAP 470P
C858	87-010-322-080		C-CAP,S 100P-50 CH
C859	87-016-459-040		CAP,E 470-10 SMG
C860	87-010-405-040		CAP,E 10-50
C861	87-010-197-080		CAP, CHIP 0.01 DM
C862	87-010-405-040		CAP,E 10-50
C863	87-010-197-080		CAP, CHIP 0.01 DM
C864	87-010-197-080		CAP, CHIP 0.01 DM
C865	87-010-197-080		CAP, CHIP 0.01 DM
C866	87-010-197-080		CAP, CHIP 0.01 DM
C891	87-010-405-040		CAP,E 10-50
C892	87-010-197-080		CAP, CHIP 0.01 DM
C893	87-010-322-080		C-CAP,S 100P-50 CH
C901	87-010-197-080		CAP, CHIP 0.01 DM
C903	87-010-197-080		CAP, CHIP 0.01 DM
C904	87-010-196-080		CHIP CAPACITOR,0.1-25
C905	87-010-196-080		CHIP CAPACITOR,0.1-25
C906	87-010-405-040		CAP,E 10-50
C931	87-010-805-080		CAP, S 1-16
C932	87-010-197-080		CAP, CHIP 0.01 DM
C933	87-010-322-080		C-CAP,S 100P-50 CH
C943	87-010-405-040		CAP,E 10-50
C944	87-010-805-080		CAP, S 1-16
C945	87-010-154-080		CAP CHIP 10P
C946	87-010-154-080		CAP CHIP 10P
C947	87-010-316-080		C-CAP,S 33P-50 CH
C948	87-010-316-080		C-CAP,S 33P-50 CH
C949	87-010-805-080		CAP, S 1-16
C952	87-010-805-080		CAP, S 1-16
C953	87-010-196-080		CHIP CAPACITOR,0.1-25
C954	87-010-196-080		CHIP CAPACITOR,0.1-25
C955	87-010-196-080		CHIP CAPACITOR,0.1-25
C956	87-010-805-080		CAP, S 1-16
C957	87-010-805-080		CAP, S 1-16
C958	87-010-805-080		CAP, S 1-16
C959	87-010-805-080		CAP, S 1-16
C960	87-010-805-080		CAP, S 1-16
C961	87-010-805-080		CAP, S 1-16
C962	87-010-805-080		CAP, S 1-16
C963	87-010-196-080		CHIP CAPACITOR,0.1-25
C991	87-010-322-080		C-CAP,S 100P-50 CH
C992	87-010-322-080		C-CAP,S 100P-50 CH
CN3	86-ZG1-609-010		CONN ASSY,6P
CN3	87-A60-133-010		CONN,8P V FE
CN6	87-A60-160-010		CONN,12P H FE
CN7	86-ZG1-606-010		CONN ASSY 2P
CN7	86-ZG1-606-010		CONN ASSY 2P
CN101	87-A60-424-010		CONN,16P V TOC-B
CN102	87-009-034-010		CONN,6P PH V
CN301	87-A60-154-010		CONN,6P H FE
CN302	86-ZG1-620-010		CONN ASSY,2P VIDEO-SW
CN851	87-A60-109-010		CONN,2P V S2M-2W

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
J851	87-009-502-010		JACK,PIN 1P Y EARTH
L101	87-005-196-080		COIL,10UH
L102	87-005-196-080		COIL,10UH
L151	87-005-204-080		COIL,47UH
L301	87-A50-095-010		COIL,68UH RCR875D
L302	87-005-469-080		COIL 4.7UH FLR50
L851	87-005-196-080		COIL,10UH
L852	87-005-466-080		COIL,2.7UH J FLR50
L853	87-005-196-080		COIL,10UH
L891	87-005-196-080		COIL,10UH
L901	87-005-196-080		COIL,10UH
L941	87-005-196-080		COIL,10UH
M601	87-045-305-010		MOTOR, RF-500TB DC-5V (2MA)
R130	87-022-364-080		C-RES,S 82K-1/10W F
R131	87-022-364-080		C-RES,S 82K-1/10W F
R132	87-022-364-080		C-RES,S 82K-1/10W F
R133	87-022-364-080		C-RES,S 82K-1/10W F
R134	87-022-364-080		C-RES,S 82K-1/10W F
R135	87-022-364-080		C-RES,S 82K-1/10W F
SW601	87-036-109-010		PUSH SWITCH
SW602	87-036-109-010		PUSH SWITCH
SW603	87-036-109-010		PUSH SWITCH
X801	87-030-270-080		VIB,XTAL 16.9344MHZ
X901	87-030-264-080		CERA LOCK(MU)12.0MHZ
X902	87-A70-145-080		VIB,CER 33.86MHZ CSTMXWOH3
X903	87-A70-152-080		VIB,CER 45.00MHZ CSAMXZ040
X904	87-A70-084-080		VIB,XTAL 13.5MHZ-50P

T-T C.B

C411	87-018-214-080		CAP TC U 0.1-50F
CON8	87-A60-156-010		CONN,8P H FE
LED411	87-070-288-010		LED,GL380
M401	87-A90-036-010		MOT ASSY,RF-300CA-11
PS401	87-A90-156-010		SNSR,SG-240
Q411	87-A30-031-010		P-TR,PT380F
S401	87-036-109-010		PUSH SWITCH

LED C.B

LED701	87-017-733-080		LED,SEL1250SMTP5 RED
LED702	87-017-733-080		LED,SEL1250SMTP5 RED
LED703	87-017-733-080		LED,SEL1250SMTP5 RED

VIDEO SW C.B<YVOS1NDM,VOS DSM>

S851	87-A90-238-010		SW,SL 1-1-3 9L

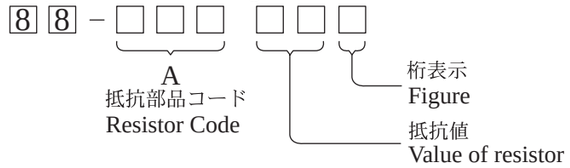
DRIVE C.B

CN3	87-009-349-010		CONN,6P H WHT PH
M20	87-045-358-010		MOT,RF-310TA 43
M21	87-045-356-010		MOT,RF-310TA 30
SW1	87-A90-042-010		SW,LEAF MSW-17310MVPO

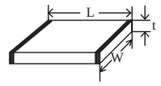
- Regarding connectors, they are not stocked as they are not the initial order items.
  The connectors are available after they are supplied from connector manufacturers upon the order is received.

○チップ抵抗部品コード／CHIP RESISTOR PART CODE

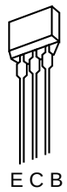
チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



チップ抵抗
Chip resistor

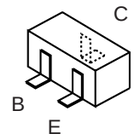
容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード : A Resistor Code : A
1/16W	1005	± 5%	CJ		1.0	0.5	0.35	104
1/16W	1608	± 5%	CJ		1.6	0.8	0.45	108
1/10W	2125	± 5%	CJ		2	1.25	0.45	118
1/8W	3216	± 5%	CJ		3.2	1.6	0.55	128

TRANSISTOR ILLUSTRATION

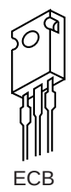


2SA933

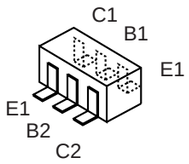
2SA1015
2SC2001
2SD655
2SD2172



2SA1162
2SC2712
DTA123JK
DTA124XK
DTC123JK
DTC124XK
DTC143TK
DTC144EK

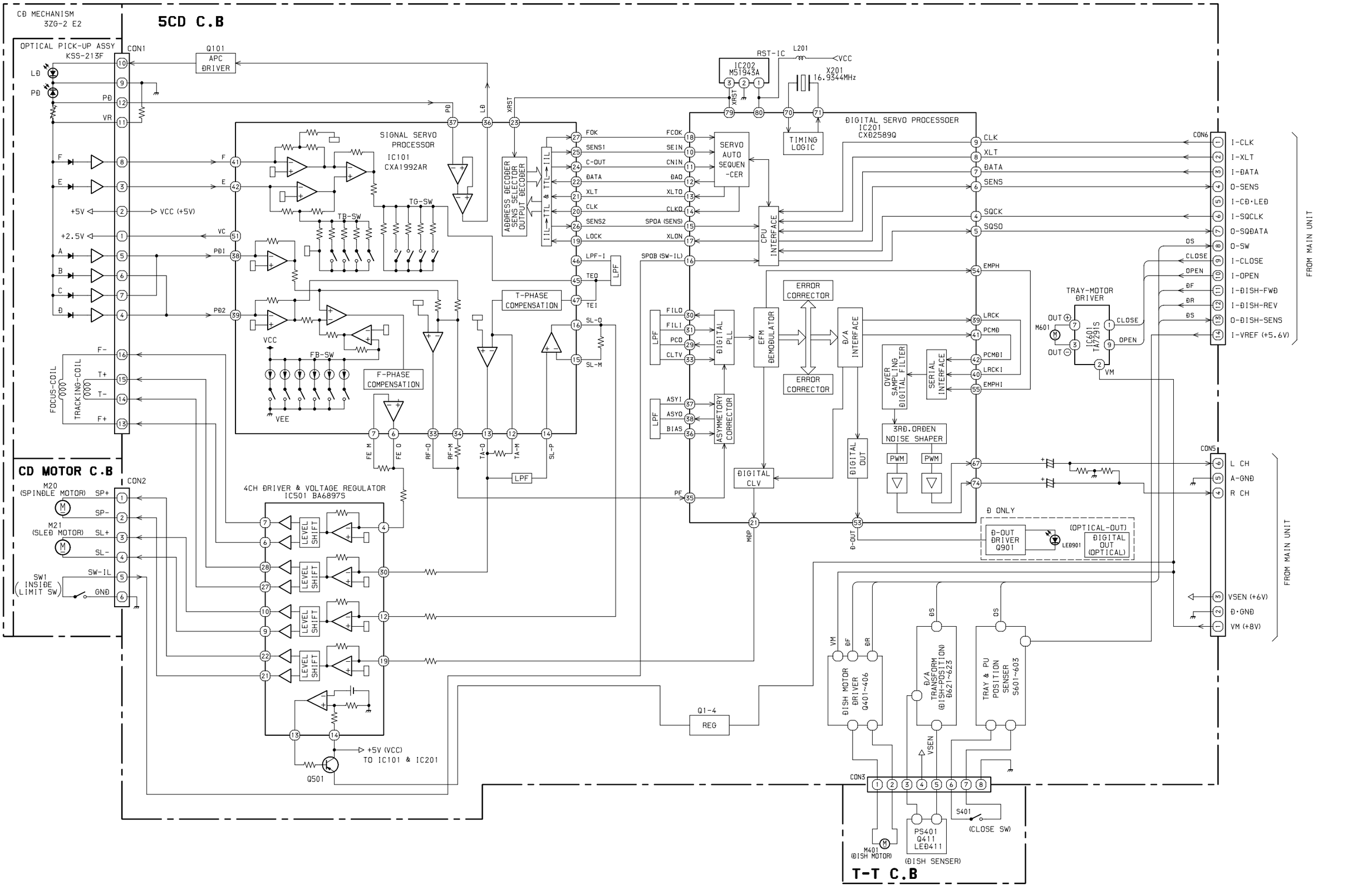


2SA1357

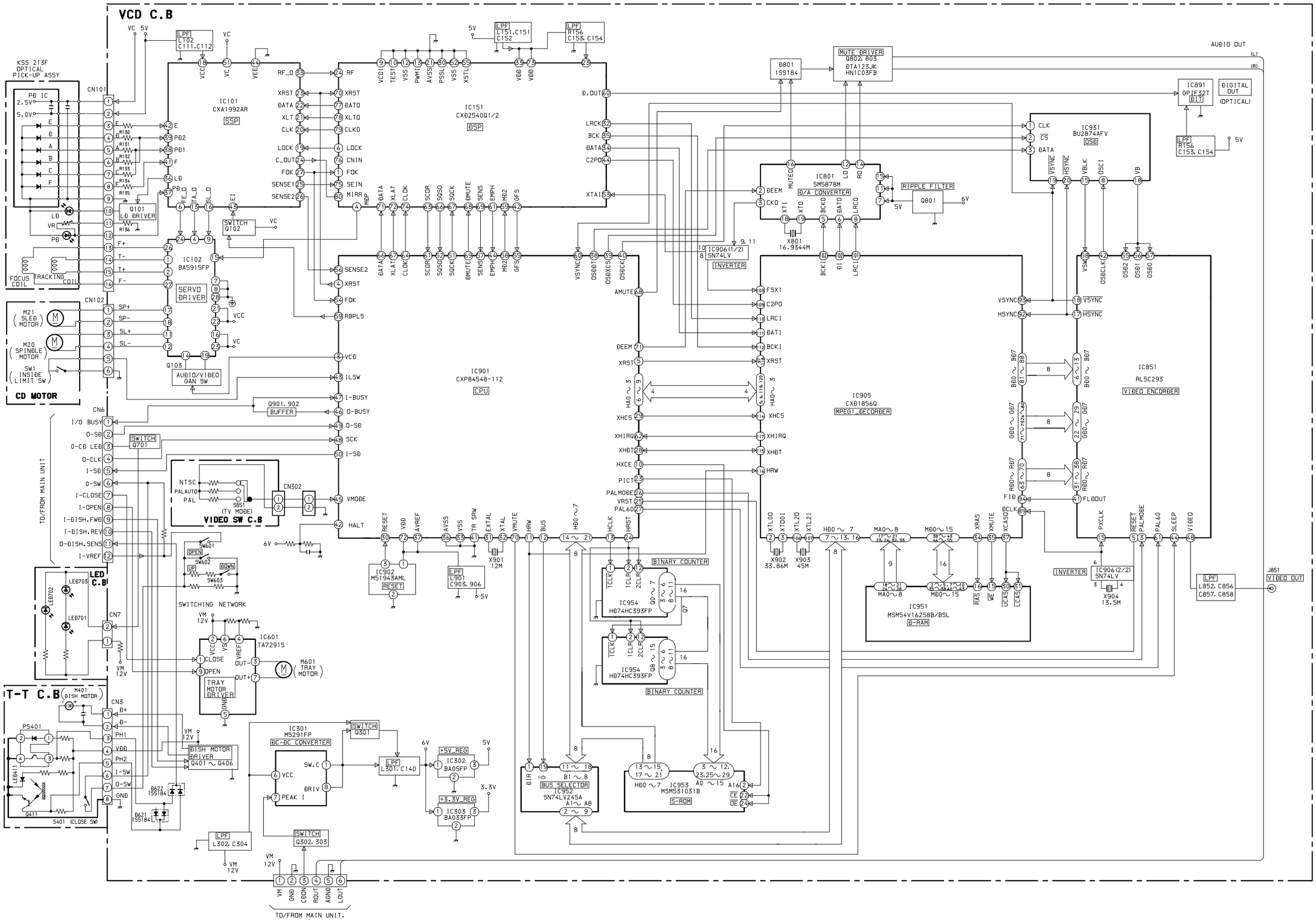


HN1C03F

BLOCK DIAGRAM-1 (YSDFNSHCM, YSDNSHM, SDFNSHM)



BLOCK DIAGRAM-2 (VOS1NDSM, YVOS1NDM)



1 2 3 4 5 6 7 8 9 10 11 12 13 14

A B C D E F G H I J K

5CÐ C.B

TO MAIN UNIT

TO CÐ MOTOR C.B
PIN3

TO PICK UP ASSY

S601
S601
(OPEN
SW)

S602
(UP SW)

M601
(TRAY
MOTOR)

CON6

IC501

IC101

CON2

CON1

IC201

IC202

IC601

W201

Q002
Q003
Q004
Q001
Q403
Q406
Q402
Q404
Q401
Q405
Q501
Q101
Q901

D622
D623
D621
D101

S603
(DOWN)
SW

CON5

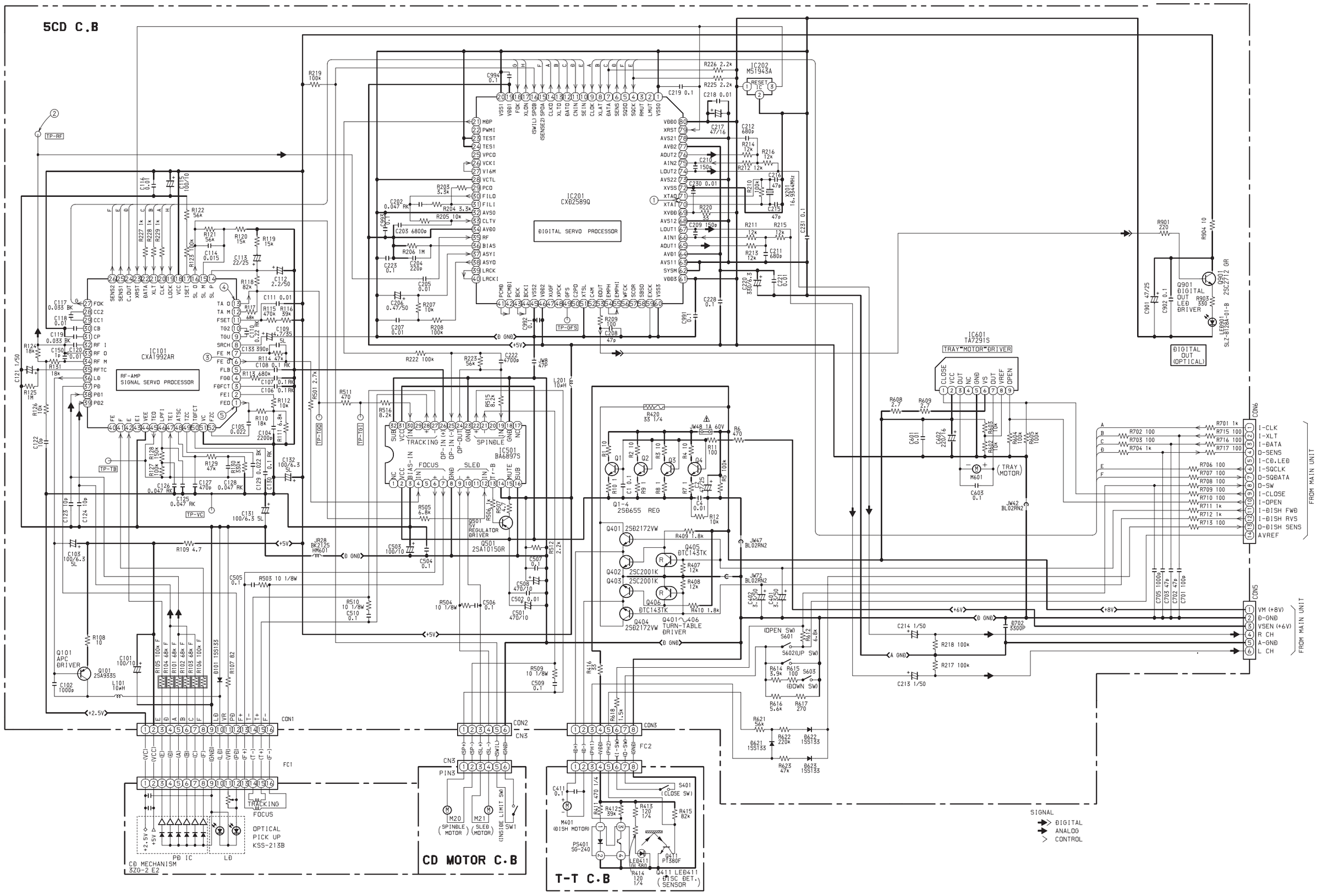
LED901

DIGITAL
OUT
(OPTICAL)

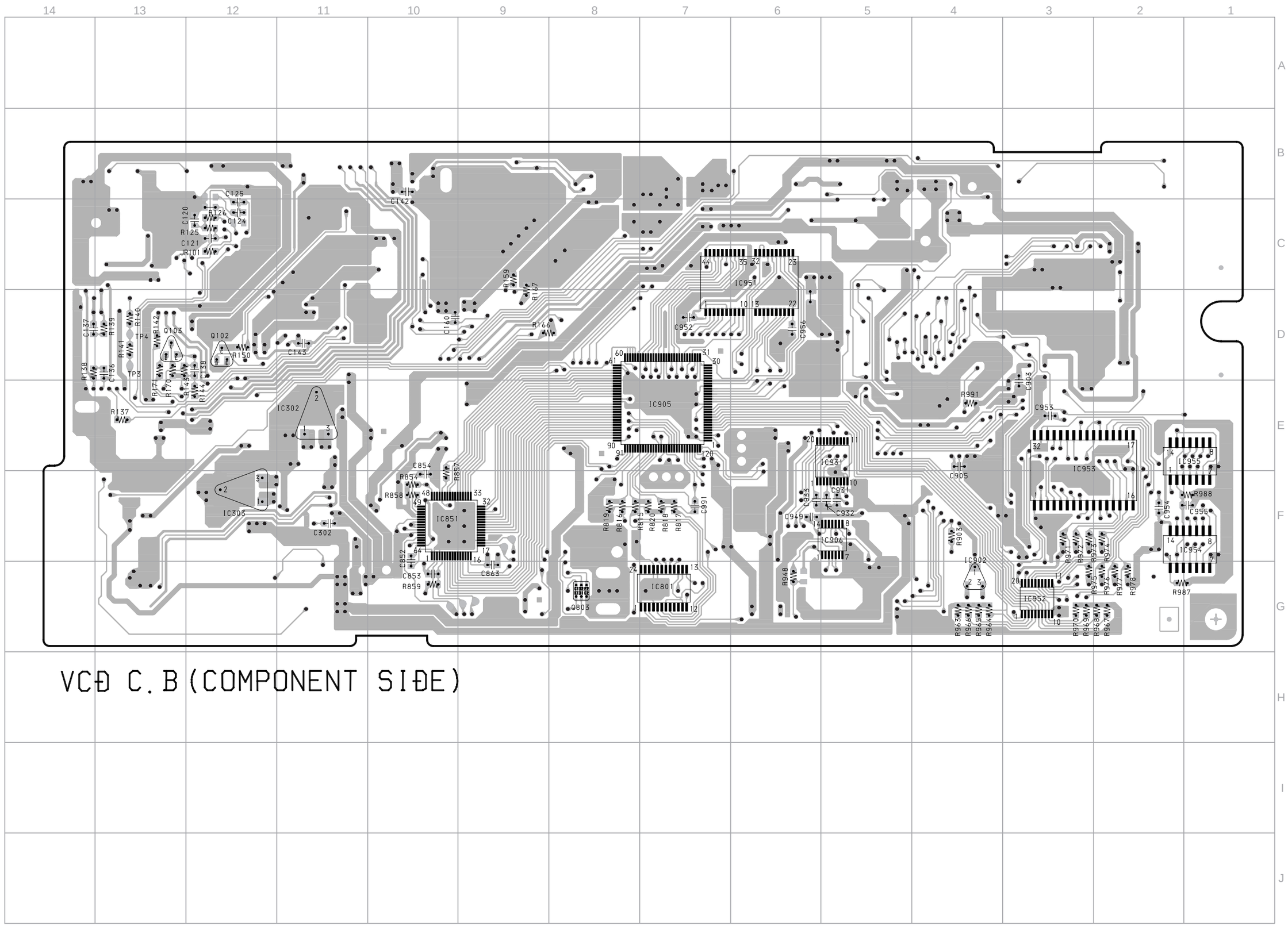
TO T-T C.B
CON8

TO MAIN UNIT

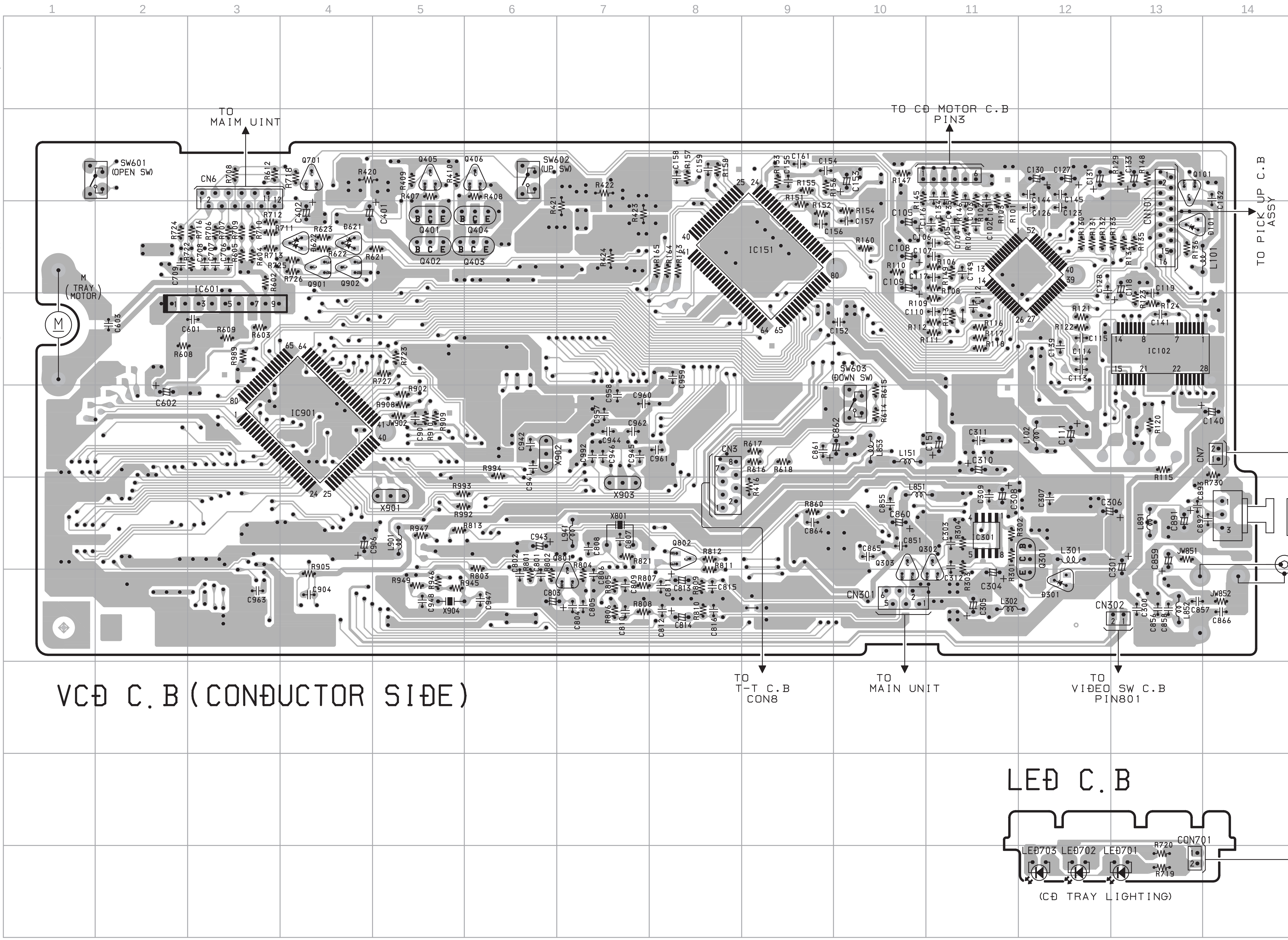
SCHEMATIC DIAGRAM-1 (YSDFNSHCM, YSDNSHM, SDFNSHM)



WIRING-2 (VOS1NDSM, YVOS1NDM)



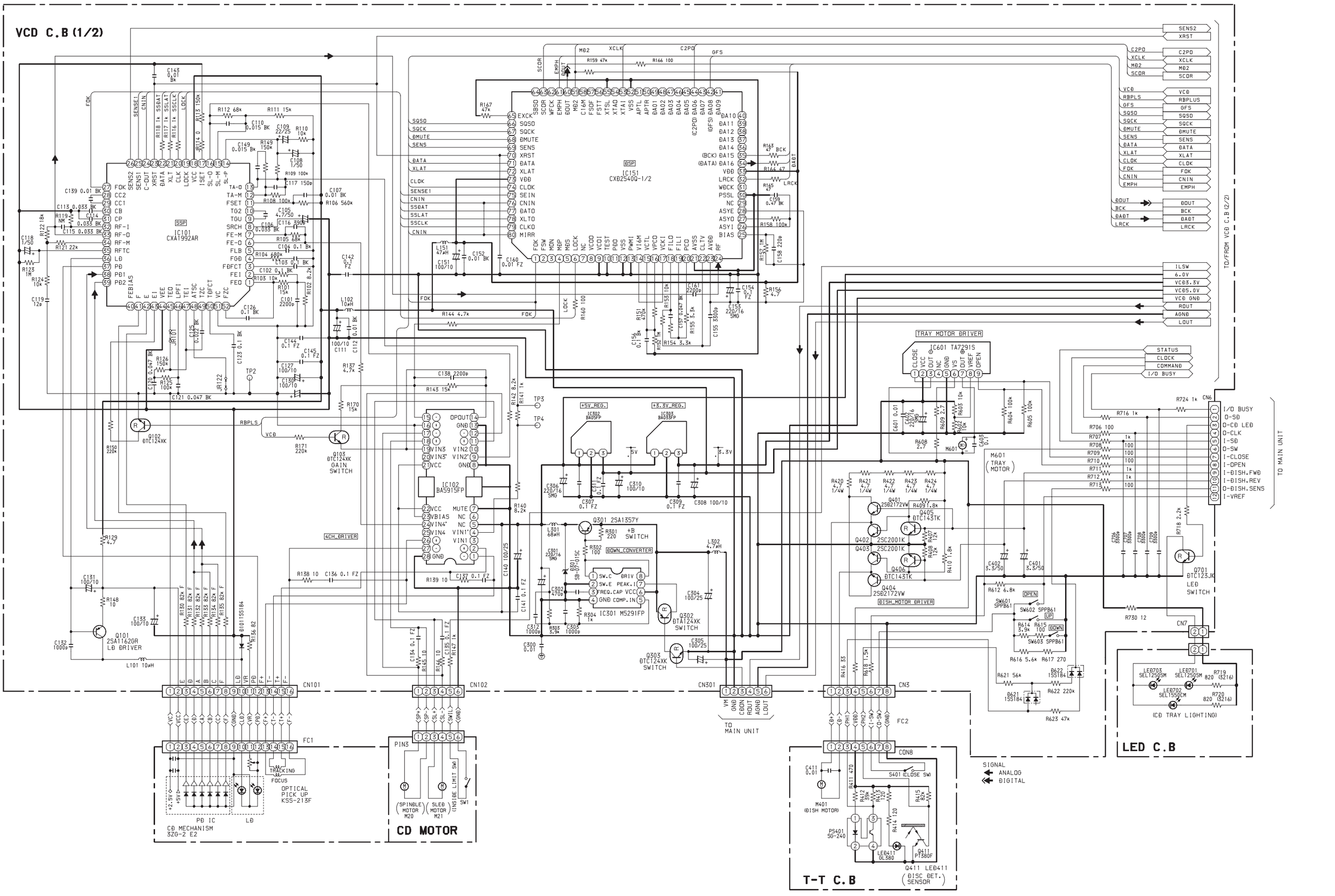
VCD C.B (COMPONENT SIDE)



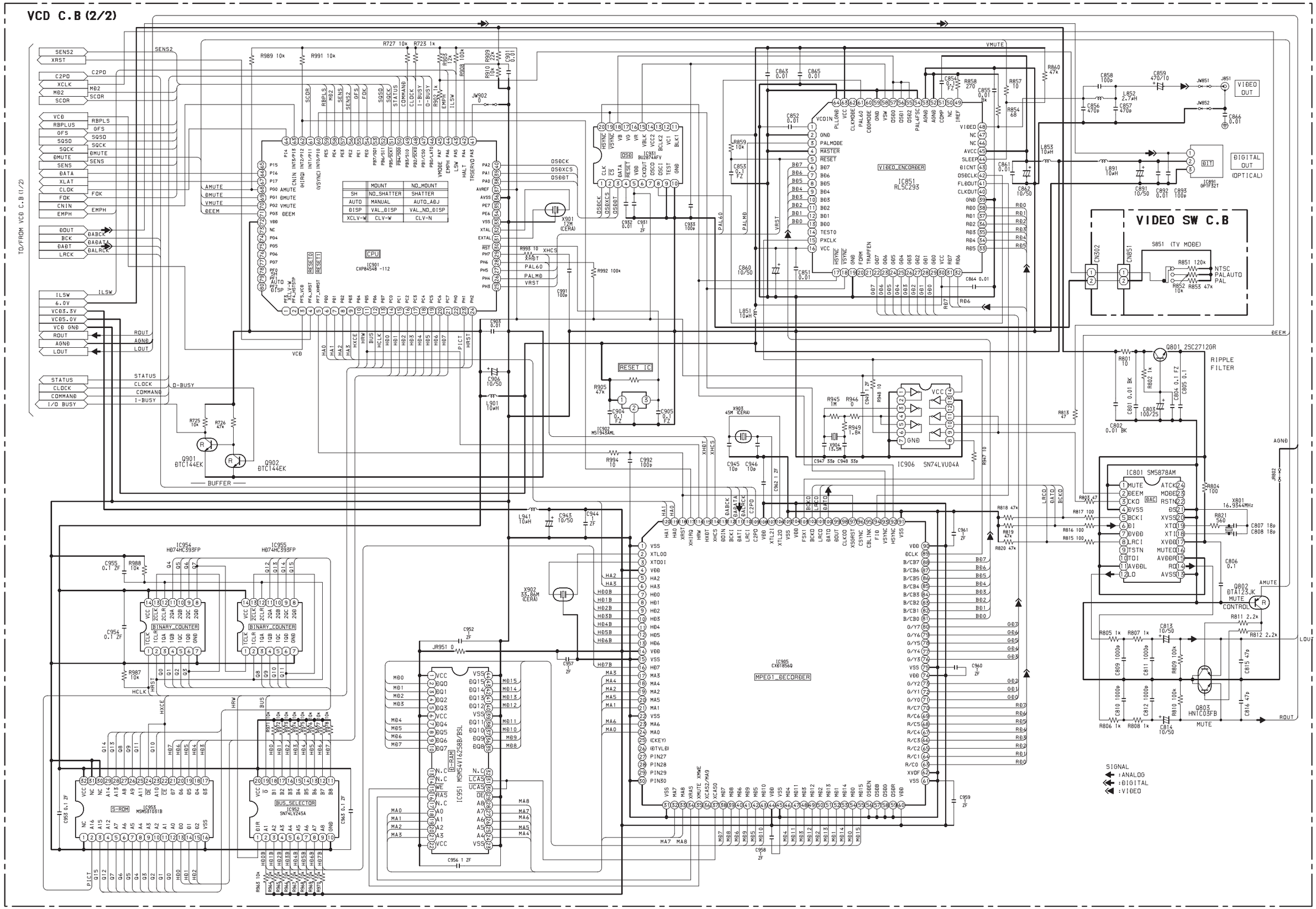
VCD C.B (CONDUCTOR SIDE)

LED C.B

SCHEMATIC DIAGRAM-2 (VOS1NDSM, YVOS1NDM 1/2)

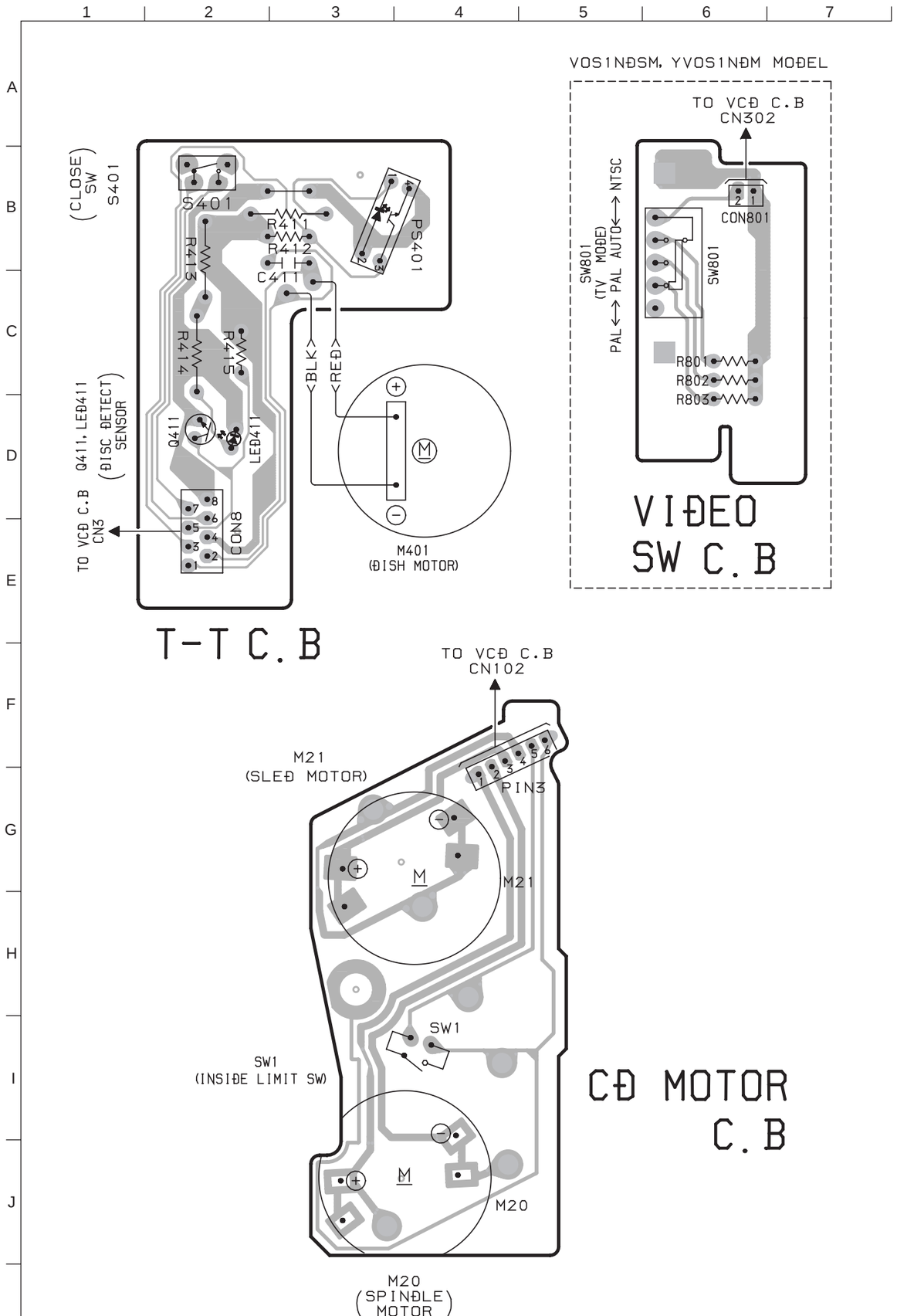


SCHEMATIC DIAGRAM-3 (VOS1NDSM, YVOS1NDM 2/2)



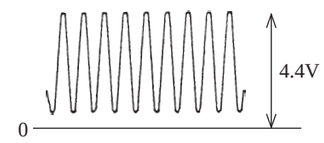
	MOUNT	NO_MOUNT
SH	NO_SHATTER	SHATTER
AUTO	MANUAL	AUTO_ADJ
DISP	VAL_DISP	VAL_NO_DISP
XCLV-W	CLV-W	CLV-N

WIRING-3

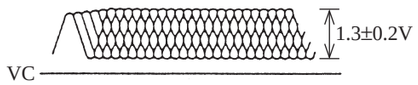


WAVE FORM

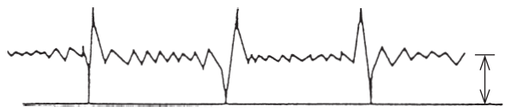
① SYSTEM CLOCK
f=16.9344MHz
VOLT/DIV: 2V
TIME/DIV: 0.1μS



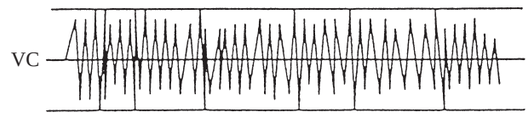
② RF
VOLT/DIV: 500mV
TIME/DIV: 0.5μS



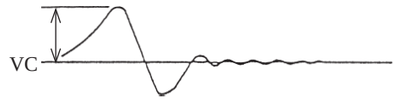
③ FOCUS
VOLT/DIV: 200mV
TIME/DIV: 2mS



④ TRACKING
TIME/DIV: 1mS

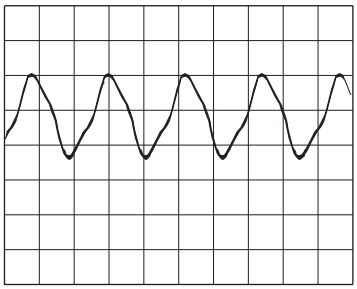


⑤ FOCUS SEARCH



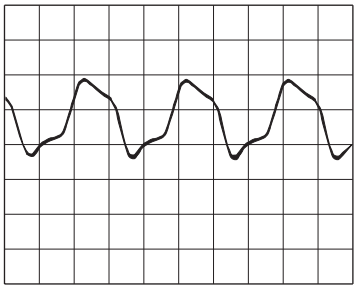
⑥ IC905 Pin ⑯⑥ (XTL20)

VOLT/DIV: 2V
TIME/DIV: 10nS



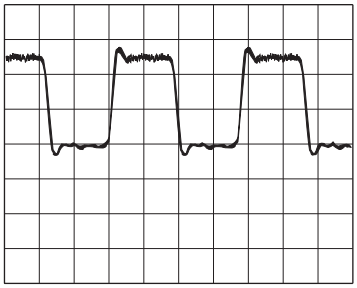
⑦ IC905 Pin ② (XTL00)

VOLT/DIV: 2V
TIME/DIV: 10nS



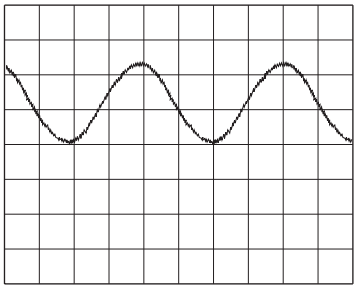
⑧ IC906 Pin ⑥

VOLT/DIV: 2V
TIME/DIV: 20nS



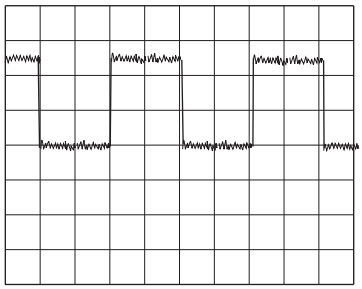
⑨ IC901 Pin ㉛ (EXTAL)

VOLT/DIV: 2V
TIME/DIV: 20nS



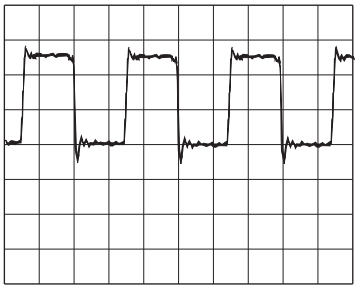
⑩ IC851 Pin ㊶ (FLDOUT)

VOLT/DIV: 2V
TIME/DIV: 10mS



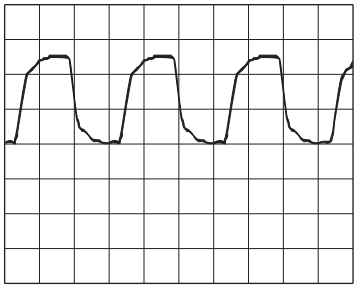
⑪ IC851 Pin ㊷ (OSDCLK)

VOLT/DIV: 2V
TIME/DIV: 50nS



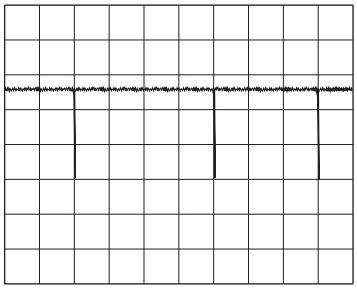
⑫ IC801 Pin ③ (CKO)

VOLT/DIV: 2V
TIME/DIV: 20nS



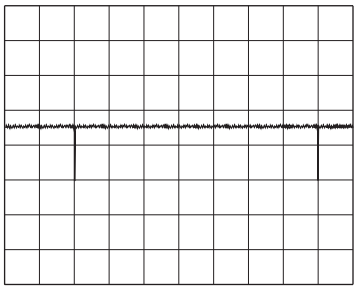
⑬ IC952 Pin ⑪ (B8)

VOLT/DIV: 2V
TIME/DIV: 1mS



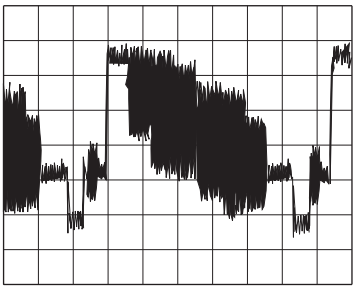
⑭ IC952 Pin ⑨ (A8)

VOLT/DIV: 2V
TIME/DIV: 1mS



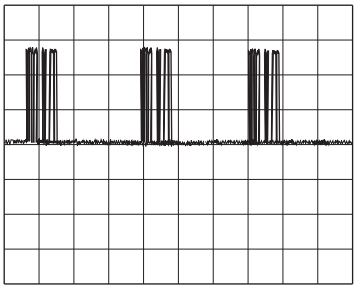
IC851 Pin ⑥① (PAL60)
PAL DISC PAL

VOLT/DIV: 200mV
TIME/DIV: 10µS



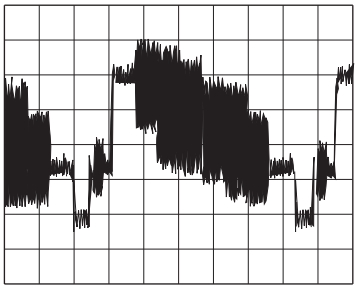
⑮ IC931 Pin ⑮ (VBLK)

VOLT/DIV: 2V
TIME/DIV: 20µS



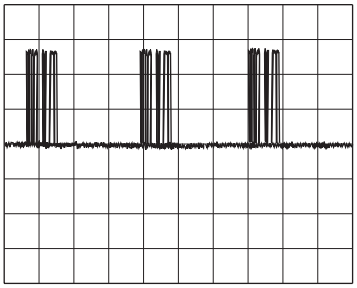
IC851 Pin ⑥① (PAL60)
NTSC DISC PAL AUTO

VOLT/DIV: 200mV
TIME/DIV: 10µS



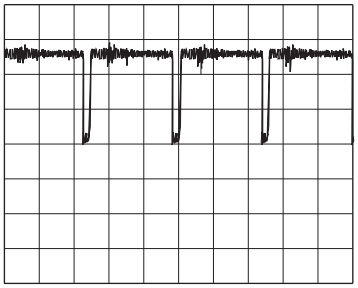
⑯ IC931 Pin ⑱ (VB)

VOLT/DIV: 2V
TIME/DIV: 20µS



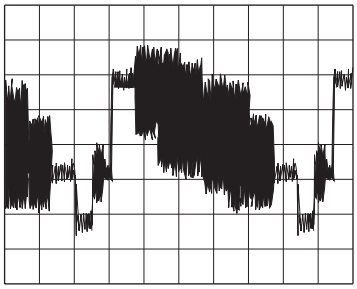
⑱ IC851 Pin ⑰ ($\overline{\text{H SYNC}}$)
NTSC

VOLT/DIV: 2V
TIME/DIV: 50µS



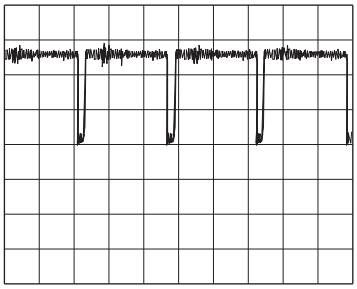
⑰ IC851 Pin ⑥① (PAL60)
NTSC DISC NTSC

VOLT/DIV: 200mV
TIME/DIV: 10µS

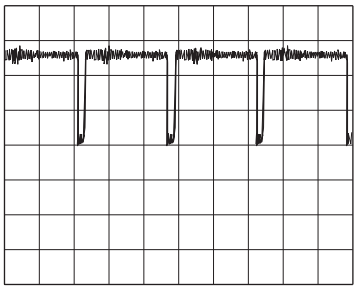


IC851 Pin ⑰ ($\overline{\text{H SYNC}}$)
PAL AUTO

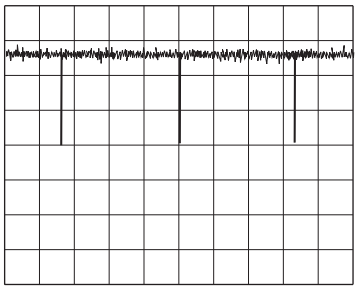
VOLT/DIV: 2V
TIME/DIV: 50µS



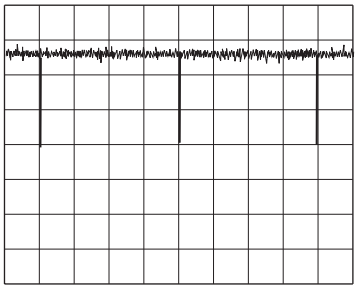
IC851 Pin ⑰ ($\overline{\text{H SYNC}}$) VOLT/DIV: 2V
PAL TIME/DIV: 50µS



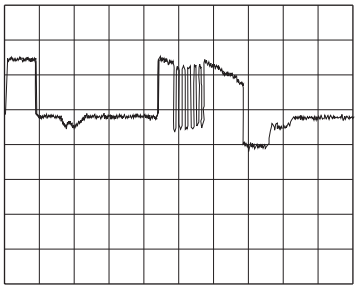
IC851 Pin ⑱ ($\overline{\text{V SYNC}}$) VOLT/DIV: 2V
PAL TIME/DIV: 10mS



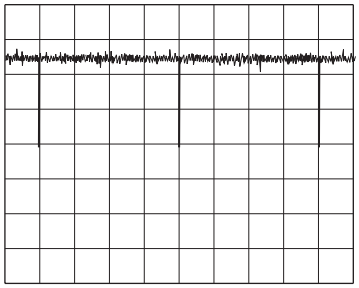
⑲ IC851 Pin ⑱ ($\overline{\text{V SYNC}}$) VOLT/DIV: 2V
NTSC TIME/DIV: 10mS



⑳ CN6 Pin ⑪ (O-DISH, SENS) VOLT/DIV: 2V
TIME/DIV: 200mS



IC851 Pin ⑱ ($\overline{\text{V SYNC}}$) VOLT/DIV: 2V
PAL AUTO TIME/DIV: 10mS



IC DESCRIPTION

IC, CXD2589Q

Pin No.	Pin Name	I/O	Description
1, 20, 45, 60	VSS	—	GND.
2	LMUT	O	Lch-“0” detect flag.
3	RMUT	O	Rch-“0” detect flag.
4	SQCK	I	Clock input for SQSO read out.
5	SQSO	O	SubQ 80 bit serial output.
6	SENS	O	SENS signal output to CPU.
7	DATA	I	Serial data input from CPU.
8	XLAT	I	Latch input from CPU, Latch serial data at fall down.
9	CLOK	I	Clock input to serial data transfer from CPU.
10	SEIN	I	SENS input from SSP.
11	CNIN	I	Numbers of track jump are counted and input.
12	DATO	O	Serial data output to SSP.
13	XLTO	O	Serial-data latch output to SSP. Latch at fall down.
14	CLKO	O	Clock output for serial data transfer to SSP.
15	SPOA	I	Microcomputer expansion interface. (Input A)
16	SPOB	I	Microcomputer expansion interface. (Input B)
17	XLON	O	Microcomputer expansion interface. (Output)
18	FOK	I	Focus OK input terminal. Used for SENS output and servo-auto sequencer.
19, 46, 61, 80	VDD	—	Power supply. (+5V)
21	MDP	O	Servo control for spindle motor.
22	PWMI	I	External control input for spindle motor.
23	TEST	I	TEST terminal. (Connected to GND)
24	TESI	I	TEST terminal. (Connected to GND)
25	VPCO	O	Charge pump output for extensive EFM PLL.
26	VCKI	I	VCO2 oscillator input for extensive EFM PLL.
27	V16M	O	VCO2 oscillator output for extensive EFM PLL.
28	VCTL	I	VCO2 control voltage input for extensive EFM PLL.
29	PCO	O	Charge pump output for master PLL.
30	FILO	O	Filter (slave = digital PLL) output for master PLL.
31	FILI	I	Filter input for master PLL.
32	AVSS	—	Analog GND.
33	CLTV	I	VCO control voltage input for master.
34	AVDD	—	Analog power. (+5V)
35	RF	I	EFM signal input.
36	BIAS	I	Constant current input to asymmetry circuit.
37	ASYI	I	Comparison voltage input to asymmetry circuit.
38	ASYO	O	EFM full-swing output. (L=VSS, H=VDD)
39	LRCK	O	D/A interface, LR clock output f=FS.
40	LRCKI	I	LR clock input.
41	PCMD	O	D/A interface, serial data output. (2’s COMP, MSB first)
42	PCMDI	I	D/A interface, serial data input. (2’s COMP, MSB first)

Pin No.	Pin Name	I/O	Description
43	BCK	O	D/A interface bit clock output.
44	BCKI	I	D/A interface bit clock input.
47	XUGF	O	XUGF output, MNT1 or RPCK output by switching command.
48	XPCK	O	XPLCK output, MNT0 output by switching command.
49	GFS	O	GFS output, MNT3 or XRAOF output by switching command.
50	C2PO	O	C2PO output, GTOP output by switching command.
51	XTSL	I	X'tal select input terminal, X'tal: 16.9344MHz = "L" 33.8688MHz = "H".
52	C4M	O	4.2336MHz output, Output 1/4 divided frequency of VCKI at CAV-W mode.
53	DOUT	O	Digital Out connector output signal.
54	EMPH	O	"H" when the playback disc has emphasis. "L" when it does not.
55	EMPHI	I	De-emphasis ON/OFF, "H" when ON, "L" when OFF.
56	WFCK	O	WFCK output.
57	SCOR	O	H output when the subcode sync S0 or S1 is detected.
58	SESO	O	Serial output for SubP-W.
59	EXCK	I	SBSO read out clock input.
62	SYSM	I	Mute input terminal, Active the "H" setting.
63	AVSS	—	Analogue GND.
64	AVDD	—	Analogue power supply. (+5V)
65	AOUT1	O	Lch/analogue output terminal.
66	AINI	I	Lch/OP AMP input terminal.
67	LOUT1	O	Lch/LINE output terminal.
68	AVSS	—	Analogue GND.
69	XVDD	—	Power supply for master clock.
70	XTAI	I	Input terminal for crystal oscillator circuit. Input external master clock from this terminal.
71	XTAO	O	Output terminal for crystal oscillator circuit.
72	XVSS	—	GND terminal for master clock.
73	AVSS	—	Analogue GND.
74	LOUT2	O	Rch/LINE output terminal.
75	AIN2	I	Rch/OP AMP input terminal.
76	AOUT2	O	Rch/analogue output terminal.
77	AVDD	—	Analogue power supply. (+5V)
78	AVSS	—	Analogue GND.
79	XRST	I	Reset system at "L" setting.

Note)

- PCMD is the two's complement output with MSB first.
- GTOP monitors the protection status of the Frame Sync. (H: Sync protection window opened).
- XUGF is the Frame Sync negative pulse which is obtained from the EFM signal. This is the signal before the sync protection.
- XPLCK is the inverted signal of the EFM PLL clock. The PLL works so that the fall-down edge and the changed point of the EFM signal agree.
- GFS is the signal that goes "H" when the Frame Sync and the internally inserted timing agree.
- RFCK is the signal having 136 micro-seconds (during normal speed) that is generated to have the same accuracy as X'tal.
- C2PO is the signal indicating the error status of the data.
- XRAOF is the signal that is generated when the 16k RAM goes outside the jitter margin ±4F.

IC, CXA1992AR

Pin No.	Pin Name	I/O	Description
1	FEO	O	Output terminal for focus error amplifier. Internally connected to window comparator input for bias condition.
2	FEI	I	Input terminal for focus error.
3	FDFCT	I	Capacitor connection terminal for time constant used when there is defect.
4	FGD	I	This pin is connected to GND via capacitor when high frequency gain of the focus servo is attenuated.
5	FLB	I	This is a pin where the time constant is externally connected to raise the low frequency gain of the focus servo.
6	FE_O	O	Focus drive output.
7	FEM	I	Focus amplifier inverted input pin.
8	SRCH	I	This is a pin where the time constant is externally connected to generate the focus search waveform.
9	TGU	I	This is a pin where the selection time constant is externally connected to set the tracking servo the high frequency gain.
10	TG2	I	This is a pin where the selection time constant is externally connected to set the tracking high frequency gain.
11	FSET	I	Pin for setting peak of the phase compensator of the focus tracking.
12	TA_M	I	Tracking amplifier inverted input pin.
13	TA_O	O	Tracking drive output.
14	SL_P	I	Sled amplifier non-inverted input pin.
15	SL_M	I	Sled amplifier inverted input pin.
16	SL_O	O	Sled drive output.
17	ISET	I	The current which determines height of the focus search, track jump and sled kick is input with external resistance connected.
18	Vcc	I	Power supply.
19	LOCK	I	“L” setting starts sled disorder-prevention circuit. (Not pull-up resistance)
20	CLK	I	Clock input for serial data transfer from CPU. (No pull-up resistance)
21	XLT	I	Latch input from CPU. (No pull-up resistance)
22	DATA	I	Serial data input from CPU. (No pull-up resistance)
23	XRST	I	Reset system at “L” setting. (No pull-up resistance)
24	C_OUT	O	Signal output for track number counting.
25	SENS1	O	FZC, DFCT1, TZC, BALH, TGH, FOH, or ATSC is output depending on the command from CPU.
26	SENS2	O	DFCT2, MIRR, BALL, TGL or FOL is output depending on the command from CPU.
27	FOK	O	Output terminal for focus OK comparator.
28	CC2	I	Input pin where the DEFECT bottom hold output is capacitance coupled.
29	CC1	O	DEFECT bottom-hold output terminal. Internally connected to interruption comparator input.
30	CB	I	Connection terminal for DEFECT bottom-hold capacitor.
31	CP	I	Connection terminal for MIRR hold-capacitor. Anti-reverse input terminal for MIRR comparator.

Pin No.	Pin Name	I/O	Description
32	RF_I	I	Input terminal by capacity combination of RF summing amplifier.
33	RF_O	O	Output terminal of RF summing amplifier. Checkpoint of Eye pattern.
34	RF_M	I	Anti-reverse input terminal for RF summing amplifier. The gain of RF amplifier is decided by the connection resistance between RF_M and RFO terminals.
35	RFTC	I	This is a pin where the selection time constant is externally connected to control the RF level.
36	LD	O	APC amplifier output terminal.
37	PD	I	APC amplifier input terminal.
38, 39	PD1, PD2	I	RFI-V amplifier inverted input pin. These pins are connected to the A+C and B+C pins of the optical pickup, receiving by currents input.
40	FEBIAS	I/O	Bias adjustment pin of the focus error amplifier.
41, 42	F, E	I	F and EIV amplifier inverted input pins. These pins are connected to the F and E of the optical pickup, receiving by current input.
43	EI	—	Gain adjustment pin of the I-V amplifier E. (When not in use of BAL automatic adjustment)
44	VEE	—	GND connection pin.
45	TEO	O	Output terminal for tacking-error amplifier. Output E-F signal.
46	LPFI	I	BAL adjustment comparator input pin. (Input through LPF from TEO)
47	TEI	I	Input terminal for tracking error.
48	ATSC	I	Window-comparator input terminal for detecting ATSC.
49	TZC	I	Input terminal for tracking-zero cross comparator.
50	TDFCT	I	Capacitor connection pin for the time constant used when there is defect.
51	VC	O	Output terminal for DC voltage reduced to half of VCC+VEE.
52	FZC	I	Input terminal for focus-zero cross comparator.

IC, CXD2540Q

Pin No.	Pin Name	I/O	Description
1	FOK	I	Focus OK input. Used for SENS output and the servo auto sequencer.
2	FSW	O	Spindle motor output filter switching output.
3	MON	O	Spindle motor on/off control output.
4	MDP	O	Spindle motor servo control.
5	MDS	O	
6	LOCK	O	High, when sampled value of GFS at 460Hz is high. Low, when sampled value of GFS at 460Hz is low by 8 times successively.
7	NC	—	Not used.
8	VCOO	O	Analog EFM PLL oscillation circuit output.
9	VCOI	I	Analog EFM PLL oscillation circuit input. fLOCK=8.6436MHz.
10	TEST	I	TEST pin.
11	PDO	O	Analog EFM PLL charge pump output.
12	VSS	—	GND.
13	PWMI	I	Spindle motor external control input.
14	V16M	O	VCO2 oscillation output for the wide-band EFM PLL.
15	VCTL	I	VCO2 control voltage input for the wide-band EFM PLL.
16	VPCO	O	Wide-band EFM PLL charge pump output.
17	VCKI	I	VCO2 oscillation input for the wide-band EFM PLL.
18	FILO	O	Multiplier PLL (slave=digital PLL) filter output.
19	FILI	I	Multiplier PLL filter input.
20	PCO	O	Multiplier PLL charge pump output.
21	AVSS	—	Analog GND.
22	CLTV	I	Multiplier VCO1 control voltage input.
23	AVDD	—	Analog power supply (5V).
24	RF	I	EFM signal input.
25	BIAS	I	Constant current input of the asymmetry circuit.
26	ASYI	I	Asymmetry comparator voltage input.
27	ASYO	O	EFM full-swing output.
28	ASYE	I	Low: asymmetry circuit off; high: asymmetry circuit on.
29	NC	—	Not used.
30	PSSL	I	Audio data output mode switching input. Low: serial output; high: parallel output.
31	WDCK	O	D/A interface for 48-bit slot. Word clock f=2Fs.
32	LRCK	O	D/A interface for 48-bit slot. LR clock f=Fs.
33	VDD	—	Power supply (5V).
34	DA16	O	DA16 (MSB) output when PSSL=1. 48-bit slot serial data (two's complement, MSB first) when PSSL=0.
35	DA15	O	DA15 output when PSSL=1. 48-bit slot bit clock when PSSL=0.
36	DA14	O	DA14 output when PSSL=1. 64-bit slot serial data (two's complement, LSB first) when PSSL=0.
37	DA13	O	DA13 output when PSSL=1. 64-bit slot bit clock when PSSL=0.
38	DA12	O	DA12 output when PSSL=1. 64-bit slot LR clock when PSSL=0.

Pin No.	Pin Name	I/O	Description
39	DA11	O	DA11 output when PSSL=1. GTOP output when PSSL=0.
40	DA10	O	DA10 output when PSSL=1. XUGF output when PSSL=0.
41	DA09	O	DA09 output when PSSL=1. XPLCK output when PSSL=0.
42	DA08	O	DA08 output when PSSL=1. GFS output when PSSL=0.
43	DA07	O	DA07 output when PSSL=1. RFCK output when PSSL=0.
44	DA06	O	DA06 output when PSSL=1. C2PO output when PSSL=0.
45	DA05	O	DA05 output when PSSL=1. XRAOF output when PSSL=0.
46	DA04	O	DA04 output when PSSL=1. MNT3 output when PSSL=0.
47	DA03	O	DA03 output when PSSL=1. MNT2 output when PSSL=0.
48	DA02	O	DA02 output when PSSL=1. MNT1 output when PSSL=0.
49	DA01	O	DA01 output when PSSL=1. MNT0 output when PSSL=0.
50	APTR	O	Aperture compensation control output. This pin outputs a high signal when the right channel is used.
51	APTL	O	Aperture compensation control output. This pin outputs a high signal when the left channel is used.
52	VSS	—	GND.
53	XTAI	I	Crystal oscillation circuit input.
54	XTAO	O	Crystal oscillation circuit output.
55	XTSL	I	Crystal selector input.
56	FSTT	O	2/3 frequency divider output for Pins 53 and 54.
57	FSOF	O	1/4 frequency divider output for Pins 53 and 54.
58	C16M	O	16.9344MHz output. (V16M output in CLV-W and CAV-W modes)
59	MD2	I	Digital-out on/off control. High: on; low: off
60	DOUT	O	Digital-out output.
61	EMPH	O	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
62	WFCK	I	WFCK (write frame clock) output.
63	SCOR	O	Outputs a high signal when either subcode sync S0 or S1 is detected.
64	SBSO	O	Sub P to W serial output.
65	EXCK	I	SBSO readout clock input.
66	SQSO	O	Sub Q 80-bit and PCM peak, level metter and internal status outputs.
67	SQCK	I	SQSO readout clock input.
68	MUTE	I	High: mute; low: release
69	SENS	—	SENS output to CPU.
70	XRST	I	System reset. Reset when low.
71	DATA	O	Serial data input from CPU.
72	XLAT	O	Latch input from CPU. Serial data is latched at the falling edge.
73	VDD	—	Power supply (5V).
74	CLOK	O	Serial data transfer clock input from CPU.
75	SEIN	I	SENS input from SSP.
76	CNIN	I	Track jump count signal input.

Pin No.	Pin Name	I/O	Description
77	DATO	O	Serial data output to SSP.
78	XLTO	O	Serial data latch output to SSP. Latched at the falling edge.
79	CLKO	O	Serial data transfer clock output to SSP.
80	MIRR	I	Mirror signal input. Used when the number of tracks is 128 or more for the 2N-track jump and M track move of the auto sequencer.

Notes)

- The 64-bit slot is an LSB first, two's complement output, and the 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µ.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

IC, SM5878M

Pin No.	Pin Name	I/O	Description
1	MUTE	I	MODE = H: Soft mute ON/OFF terminal. (Mute at H). MODE = L: Attenuator level DOWN/UP terminal. (DOWN at H).
2	DEEM	I	De-emphasis ON/OFF terminal. (De-emphasis ON at H).
3	CKO	O	Oscillator clock output. (16.9344 MHz).
4	DVSS	—	Digital VSS terminal.
5	BCKI	I	Bit clock input terminal.
6	DI	I	Serial data input terminal.
7	DVDD	—	Digital VDD terminal.
8	LRCI	I	Sample rate clock (fs) input terminal. (H = L ch/L = R ch).
9	TSTN	I	Test input. (“H” or open during normal operation)
10	TO1	O	Test output 1. (Normally low level output).
11	AVDDL	—	Analog VDD terminal. (For L ch).
12	LO	O	Left channel analog output terminal.
13	AVSS	—	Analog VSS terminal.
14	RO	O	Right channel analog output terminal.
15	AVDDR	—	Analog VDD terminal. (For R ch).
16	MUTEO	O	Infinity zero detection output.
17	XVDD	—	X’tal system VDD terminal.
18	XTI	I	X’tal oscillator terminal. (Or external clock input terminal of 16.9344 MHz).
19	XTO	O	X’tal oscillator terminal.
20	XVSS	—	X’tal system VSS terminal.
21	DS	I	Double-speed/normal playback selection. (Double-speed at H).
22	RSTN	I	Reset terminal. (Reset at L).
23	MODE	I	Soft mute/Attenuator mode selection. (Soft mute at H).
24	ATCK	I	Attenuator level setup clock (Ignored when MODE = H).

IC, CXD1856R

Pin No.	Pin Name	I/O	Description
1	VSS	—	GND.
2, 3	XTL0O, XTL0I	O/I	Video decoder master clock. Input the clock signal to the XTL0I or connect an external oscillator between XTL0I and XTL 0O. The recommend frequency is 27 MHz, 28.3636 MHz (NTSC 8fs) or 65.4686 MHz (PAL 8fs).
4	VDD	—	Power supply.
5, 6, 119, 120	HA0-HA3	I	This is the register address input terminal when the host interface is in the parallel mode. HA0 is the serial data input terminal in the serial mode. HA1 to HA3 must be fixed to the “L” level during the serial mode.
7-13, 16	HD0-HD7	I/O	This is the register data input/output terminal when the host interface is in the parallel mode. HA0 is the serial data output terminal in the serial mode. HD1 to HD7 must be fixed the “L” level during the serial mode.
14	VDD	—	Power supply.
15	VSS	—	GND.
17-21, 23, 24, 32, 33	MA0-MA8	O	DRAM address signal output terminal. The DRAM address signal output terminal must be connected to the DRAM address terminal in the way that the terminal numbers match each other.
22	VSS	—	GND.
25	CKEY	O	Chroma key signal terminal. This terminal goes to “L” while outputting the color that is specified as the key color. Set this terminal to OPEN when it is not used.
26	DTVLD	O	Video data identification signal terminal. This terminal goes to “H” outputting the picture of the frame memory. This terminal goes to “L” while outputting the border color or during blanking. Set this terminal to OPEN when it is not used.
27-29	PIN27-PIN29	—	Not used.
30	PIN30	—	GND.
31	VSS	—	GND.
34	XRAS	O	Low address strobe signal output terminal. Connect this terminal to the DRAM $\overline{\text{RAS}}$ signal terminal.
35	XMWE	O	DRAM write enable signal output terminal. Connect this terminal to the DRAM $\overline{\text{WE}}$ signal terminal.
36	XCAS2/MA9	O	Use this terminal when 8-Mbit DRAM is connected. Connect this terminal to the DRAM $\overline{\text{CAS}}$ signal terminal of the upper words (256K to 512K-1) side when the DRAM system consists of the two DRAMs × 256 × 16 bits (upper bite and lower bite are common). Connect this terminal to the MA9 terminal (common to the two DRAMs) when DRAM system consists of the two DRAMs × 512 Kw × 8 bits.
37	XCAS0	O	This is the DRAM column address strobe signal output. Connect this terminal to the DRAM $\overline{\text{CAS}}$ signal terminal of the lower words (0 to 256 K-1) side when DRAM system consists of the two DRAMs × 256 Kw × 16 bits (upper bite and lower bite are common). Connect this terminal commonly to the DRAM $\overline{\text{CAS}}$ signal terminal in all connections other than the above described connection.
38-43, 46-55	MD0-MD15	I/O	DRAM data signal input/output terminal. These terminals must be connected to the DRAM data terminals in the way that the terminal numbers match each other.
44	VDD	—	Power supply.

Pin No.	Pin Name	I/O	Description
45	VSS	—	GND.
56	OSDEN	I	OSD enable signal terminal. Polarity to enable the OSD can be changed by setting the register.
57-59	OSDB, OSDG, OSDR	I	OSD data input terminal. The color that is registered in the color table and specified by the three inputs (3 bits), is output when the signal that is input to the OSDEN terminal is in the enable state.
60	VDD	—	Power supply.
61	VSS	—	GND.
62	XVOE	I	Video output enable signal terminal. When this terminal is set to “L”, the picture data output and the DCLK output are enabled. When this terminal is set to “H”, they are disabled (high impedance). In order to make the output enable, the setting of the output control register must also be set to the enable state.
63-70	R/Cr0-R/Cr7	O	Picture data output terminal. Output data formats (RGB, YCbCr) and correspondence between terminals and output data can be changed by the register setting.
71-73, 76-80	G/Y0-G/Y2, G/Y3-G/Y7	O	
81-88	B/Cb0-B/Cb7	O	
74	VDD	—	Power supply.
75	VSS	—	GND.
89	DCLK	I/O	Dot clock (DCLK) signal terminal. The DCLK frequency is normally 13.5 MHz. The DCLK signal can be input from this terminal or can be output from this terminal after dividing-frequency of the clock input.
90	VDD	—	Power supply.
91	VSS	—	GND.
92	HSYNC	I/O	Horizontal sync signal terminal. When the internal sync generator is used, the horizontal sync signal that is obtained by frequency-dividing the dot clock (DCLK) is output. When the internal sync generator is not used, the external horizontal sync is input to this terminal.
93	VSYNC	I/O	Vertical sync signal terminal. When the internal sync generator is used, the vertical sync signal that is obtained by frequency-dividing the dot clock (DCLK) is output. When the internal sync generator is not used, the external vertical sync is input to this terminal.
94	FID/FHREF	I/O	This terminal is used for the two signals of the field identification signal (FID) and the horizontal sync phase reference signal (FHREF). Use of this terminal is determined by the register setting. When set to FID, this terminal is used as output terminal when the internal sync generator is used, and is used as input terminal when the internal sync generator is not used. “H” correspond to the odd fields. When this terminal is set to FHREF, the horizontal sync phase reference signal that is obtained by frequency-dividing XTL0, is output. When XTL0 is 8 fsc, the signal that corresponds to H. SYNC cycle is generated that can be used for phase comparison with the H. SYNC signal.

Pin No.	Pin Name	I/O	Description
95	CBLNK/FSC	I/O	This terminal is used for the two signals of the composite blanking signal (CBLNK) and the fsc signal. Use of this terminal is determined by the register setting. When set to CBLNK, this terminal is used as output terminal when the internal sync generator is used, and is used as input terminal when the internal sync generator is not used. When set to fsc, the signal that is obtained by dividing-frequency of XTL0 is output. The dividing ratio of either 1/8 or 1/16 can be selected.
96	CSYNC	O	Composite sync signal terminal. The composite sync signal is generated by frequency-dividing the DCLK signal. This terminal cannot accept any inputs.
97	XSGRST	I	Sync signal generator reset signal input. The internal generator is initialized by setting this terminal to “L”.
98	CLK0O	O	The clock signal that is obtained by frequency-dividing XTL0 is output from this terminal. Dividing ratio of either 1, 1/2, 1/4 or 1/8 can be selected.
99	DOUT	O	Audio digital output terminal.
100	DATO	O	Audio serial data output terminal to DAC.
101	LRCO	O	L/R clock output terminal to DAC.
102	BCKO	O	Bit clock output terminal to DAC.
103	FSXI	I	Clock input for audio interface. Input the 256fs (11.2896 MHz), 384fs (16.9344 MHz), 512fs (22.5792 MHz) or (33.8688 MHz) etc., to this terminal.
104	VDD	—	Power supply.
105	VSS	—	GND.
106, 107	XTL2O, XTL2I	O/I	Master clock terminal of the CD-ROM decoder and audio decoder. Either input the clock signal to XTL2I or connect an external oscillator between XTL2I and XTL2O. Recommended frequency is 45 MHz. This clock serves for internal circuit only, and is not synchronized with the input and output signals.
108	VDD	—	Power supply.
109	C2PO	I	This is the terminal to input the C2 pointer from CD-DSP. It indicates that the DATI input has an error.
110	LRCI	I	This is the terminal to input the LR clock from CD-DSP. It indicates if it is L channel or R channel.
111	DATI	I	This is the terminal to input the serial data from CD-DSP.
112	BCKI	I	This is the terminal to input the bit clock from CD-DSP. This is the clock to strobe the DATI input.
113	DOIN	I	This is the terminal to input the digital data from CD-DSP.
114	XHCS	I	This is the terminal of the chip select input signal during register access.
115	XHDT	I/O	This is the terminal to output the wait signal during register access. This terminal outputs the unique wait signal that is generated or not generated by the register, during DRAM access when the host interface is in the parallel mode. The pull up resistor is required since this terminal operates in the open drain configuration. Use the pull up resistor in the serial mode operation too.
116	HRW	I	This terminal receives the R/$\overline{W}$ input signal when the host interface is in the parallel mode. This terminal receives the serial clock input during the serial mode.

Pin No.	Pin Name	I/O	Description
117	XHIRQ	O	This is the interrupt request signal output terminal. The pull up resistor is required since this terminal operates in the open drain configuration.
118	XRST	I	This is the hardware reset signal input terminal. All operations are initialized when this terminal is set to “L”.

Pin No.	Pin Name	I/O	Description
1	VCOIN	I/O	Charge pump output/VCO input terminal (Connect an external capacitor for loop filter, to this terminal).
2, 19, 39, 59	GND	—	Digital ground.
3	PALMODE	I	Video mode selection control terminal (LVTTL level). NTSC mode when PALMODE = 0. PAL mode when PALMODE = 1.
4	MASTERB	I	Video sync mode selection control terminal (LVTTL level). Internal sync mode when MASTERB = 0. External sync mode when MASTERB = 1. However, when CDGMODE = 1, mode is fixed to the external sync mode regardless of MASTERB status so that the MASTERB terminal functions the switch selecting either 262 (NTSC) or 312 (PAL) scanning line when MASTER B = 1, or 263 (NTSC or 313 (PAL) scanning line when MASTER B = 0, in the non-interlaced scanning. (See page 10) (This terminal has the pull-up function).
5	RESETB	I	Reset input terminal (LVTTL level). Enter the reset state when this terminal is set to "L".
6-13	B7-B0	I	The data B input terminal (LVTTL level). Data input range is from 16 to 235, or from 0 to 255 (as controlled by the DICNT terminal) When FORM = 0, connect this terminal to ground.
14	TESTI0	I	Test input terminal Enters the test mode when TESTI0 = 1. Connect this terminal to ground or set it open.
15	PXCLK	I	Pixel clock input terminal (LVTTL level). When inputting the pixel clock, select the input pixel clock frequency that is appropriate for the respective modes. (See page 7.) Frequency accuracy of the subcarrier signal of the video signal depends on that of this clock signal. Therefore, determine the frequency accuracy of the pixel clock according to the required accuracy of the subcarrier signal.
16, 30, 63	VCC	—	Digital block power supply (+3.3 V or +5 V).
17	HSYNCB	I/O	Horizontal sync signal input/output terminal (LVTTL level). This terminal functions as the input terminal during the external sync mode, and as the output terminal during the internal sync mode. During the external sync mode, the input sync signal is sampled by PXCLK and only the fall-down edge is detected. The standard cycle of HSYNCB is 858 clock (VCD_NTSC) or 864 clock (VCD_PAL). (For CDG mode, see page 9.) This terminal functions as the output terminal during the internal sync mode.
18	VSYNCB	I/O	Vertical sync signal input/output terminal (LVTTL level). This terminal functions as the input terminal during the external sync mode, and as the output terminal during the internal sync mode. During the external sync mode, the input sync signal is sampled by PXCLK and the fall-down edge is detected. When the fall-down edges of HSYNCB and VSYNCB agree, the timing is judged to be the start of the ODD field. When they do not agree, the timing is judged to be the start of the EVEN field. This terminal functions as the output terminal during the internal sync mode.
20	FORM	I	Input format selection terminal (LVTTL level). When FORM = 0, the input format is CCIR-601YCbCr (4 : 2 : 2) . When FORM = 1, the input format is RGB input. (This terminal has the pull-up function).

Pin No.	Pin Name	I/O	Description
21	TRAPFEN	I	Internal trap filter control terminal (LVTTL level). Trap filter display is disabled when TRAPFEN = 0. Trap filter is enabled when TRAPFEN = 1. (This terminal has the pull-up function).
22-29	G7-G0	I	The G data or Y data input terminal (LVTTL level). The data input range is from 16 to 235 or from 0 to 255 in the case of the G data (as controlled by the DICNT terminal), and the data input range is from 16 to 235 in the case of the Y data.
31-38	R7-R0	I	The R data or CbCr data input terminal (LVTTL level). The data input range is from 16 to 235 or from 0 to 255 in the case of the R data (as controlled by the DICNT terminal), and the data input range is from 16 to 240 in the case of the CbCr data.
40	CLKOUT	O	Clock output terminal Clock output of the doubled frequency of PXCLK when CLKMODE = 0. Clock output of 1/2 the frequency of PXCLK when CLKMODE = 1.
41	FLDOUT	O	Field indication signal output terminal Outputs “H” when the field is the ODD field. Outputs “L” when the field is the EVEN field. Polarity of the terminal becomes invalid during the external sync mode.
42	OSDCLK	O	Clock output terminal for OSD_IC The clock signal having 1/2 the frequency of the input PXCLK frequency is output when CLKMODE = 0. The clock signal having 1/4 the frequency of the input PXCLK frequency is output when CLKMODE = 1. (See page 6.)
43	DICNT	I	The video data input control terminal (LVTTL level). Set this terminal to DICNT = 0 normally. When DICNT = 1 is set, the data input range of RGB can be expanded to the range of 0 to 255 on the condition that FORM = 0. When FORM = 1, the Cb data can be input starting from the odd cycle. (See page 8.) (This terminal has the pull-up function).
44	SLEEP	I	The SLEEP mode control terminal (LVTTL level). Normal operation mode is selected when SLEEP = 0. The SLEEP mode is selected when SLEEP = 1.
45	AVCC	—	Analog block power supply (+5 V).
46, 47, 50	NC	—	Be sure to set this terminal to open.
48	VIDEO	O	Analog video output terminal (This terminal is driven in 37.5 Ω).
49	IREF	—	An external resistor is connected to this terminal, that sets the full scale output current value.
51	COMP	—	An external de-coupling capacitor is connected to this terminal, that is used for phase compensation.
52, 53	AGND	—	Analog ground.
54	PAL4FSC	I	CDG_PAL4FSC mode selection control terminal. (LVTTL level). Status of this PAL4FSC terminal is made valid only when PALMODE = 1 and CDGMODE = 1. The mode is the CDG_PAL908fH mode when PAL4FSC = 0. The mode is the CDG_PAL4FSC mode when PAL4FSC = 1.
55-57	OSD2-OSD0	I	The input terminal to specify the OSD color. (LVTTL level). This input signal sampled by PKCLK and is encoded instead of the data supplied from the RGB input terminal when VSW = 1. When the OSD function is not used, connect this terminal to ground.

Pin No.	Pin Name	I/O	Description
58	VSW	I	The OSD background video control terminal. (LVTTL level). This input signal sampled by PXCLK and displays the data that is supplied from the RGB input terminal when VSW = 0, and displays the data that is supplied from the OSCD 0-2 input terminal when VSW = 1.
60	CDGMODE	I	The CDG mode selection control terminal. (LVTTL level). The VCD mode is selected when CDGMODE = 0. The CDG mode is selected when CDGMODE = 1. (See page 9.) (This terminal has the pull-up function).
61	PAL60	I	The PAL60 mode selection control terminal. (LVTTL level). Set this terminal to PAL60 = 0 normally. The PAL60 mode is selected when PALMODE = 1 and PAL60 = 1 at the same time. The setting of PALMODE = 0 and PAL60 = 1 is reserved. (See page 9.) (This terminal has the pull-up function).
62	CLKMODE	I	The pixel rate frequency input selection terminal. (LVTTL level). The pixel rate frequency is input to the PXCLK terminal when CLKMODE = 0. The double pixel rate frequency is input to the PXCLK terminal when CLKMODE = 0. (See page 7.) (This terminal has the pull-up function).
64	PLLGND	—	PLL ground.

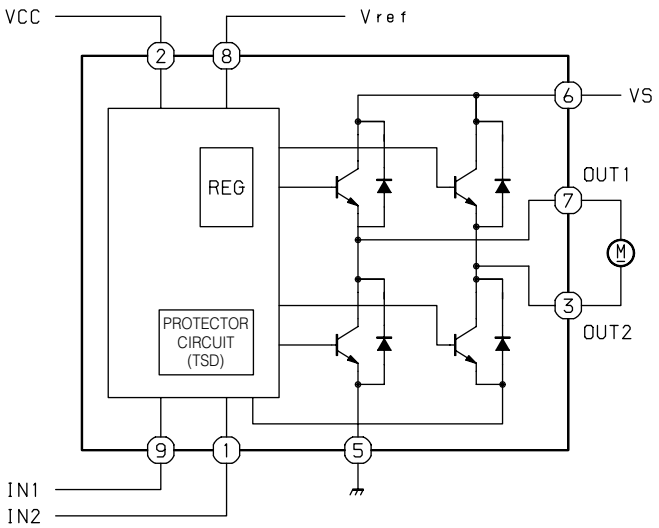
IC, CXP84548-112Q

Pin No.	Pin Name	I/O	Description
1	CLV-W	I	Fixed to CLV-W: 1, CLV-N.
2	HSTSTP	O	Cause of STOP. 1: STOP by the stop request from the host.
3	VCD	O	DISC type. 1: When no in the VCD DISC
4	XRST	O	SSP/DSP reset output. Reset at “L”.
5	XHRST	O	CXD1856 reset output. Reset at “L”.
6	HA0	O	Title back: Connected to CXD1856 HA0.
7	HA1	O	Title back: Connected to CXD1856 HA1.
8	HA2	O	Title back: Connected to CXD1856 HA2.
9	HA3	O	Title back: Connected to CXD1856 HA3.
10	HXCE	O	Connected to title back ROM XCE.
11	HRW	O	Connected to bus select DIR, CXD1586 HRW.
12	BUS	O	Connected to bus select XG.
13	HCLK	I/O	Clock for address count.
14	HD0	I/O	Title back bus data 0.
15	HD1	I/O	Title back bus data 1.
16	HD2	I/O	Title back bus data 2.
17	HD3	I/O	Title back bus data 3.
18	HD4	I/O	Title back bus data 4.
19	HD5	I/O	Title back bus data 5.
20	HD6	I/O	Title back bus data 6.
21	HD7	I/O	Title back bus data 7.
22	PH0	O	Not used.
23	PICT	O	Title back bank select. (Connected to A16).
24	HRST	O	Address counter RST output.
25	VRST	O	RL5C293 reset output. Reset at “L”.
26	PALMD	O	PAL mode output. NTSC: L, PAL: “H”.
27	PAL60	O	PAL mode output. H: PAL60 (used together with PALMD: H)
28	XHDT	I	Connected to CXD1856 XHDH.
29	XHCS	O	Connected to CXD1856 XHCS.
30	XRST	I	Reset input.
31	EXTAL	I	External 12 MHz ceramic oscillator is connected to this terminal.
32	XTAL	O	External 12 MHz ceramic oscillator is connected to this terminal.
33	VSS	I/O	Connected to ground.
34	PE6	O	Not used.
35	PE7	O	Not used.
36	AVSS	—	GND.
37	AVREF	—	3.3 V power supply.
38	OSDDT	O	OSD serial, data output.
39	OSDXCS	O	OSD serial, CS output.
40	OSDCLK	O	OSD serial, clock output.
41	TRSRVO	I	Tracking servo ON/OFF. 1: ON, 0: OFF.

Pin No.	Pin Name	I/O	Description
42	HALT	I	HALT input. 1: HALT detected (A/D conversion value is 80 H or higher).
43	LSW	I	Pick up inside switch input. “L” when INSIDE is detected.
44	EMPH	I	Emphasis input. ON only (CD-DA) at “H”.
45	VMODE	I	NTSC/PAL AUTO/PAL selection. (Analog input).
46	O-BUSY	O	Busy input to host microprocessor.
47	I-BUSY	I	Busy output from host microprocessor.
48	CLOCK	I	Host microprocessor, clock input.
49	COMMAND	I	Host microprocessor, data input.
50	STATUS	O	Host microprocessor, data output.
51	SQCK	O	Clock output for reading SQSO.
52	SQSO	I	Inputs such as SUBQ, PCM, DATA, level data, status and others.
53	PB7/SO1	O	Not used.
54	FOK	I	FOK input.
55	GFS	I	GFS input.
56	SENS2	I	SENS 2 input.
57	SENS	I	DSP SENS input.
58	MD2	O	DSP DIGITAL OUT MUTE output. ON at “H”.
59	RBPLS	O	Tracking balance fraction data output. (A+B)/2.
60	VSYNC	I	V. SYNC input.
61	SCOR	I	Subcode sync input. “H” during S0,S1 input.
62	HIRQ	I	Connected to CXP1856 HIRQ.
63	CNIN	I	C input.
64	CLOK	O	Clock output to CD DSP.
65	P15	O	Not used.
66	DATA	O	Data output to CD DSP.
67	XLAT	O	XLAT output to CD DSP.
68	AMUTE	O	LINE OUT MUTE output. Mute at “H”.
69	DMUTE	O	DSP mute output. Mute at “H”.
70	VMUTE	O	RL5C293 sleep output. Normally “L” / Sleep at “H”.
71	DEEM	O	Deemphasis output. Deemphasis ON at “H”.
72	VDD	—	3.3 V power supply.
73	NC	—	Not used.
74	PG4	O	Not used.
75	PG5	O	Not used.
76	PG6	O	Not used.
77	PG7	O	Not used.
78	SH	I	Pick that is equipped with shutter. 1: With shutter.
79	AUTO	I	Auto adjustment YES/NO. 1: Auto adjustment YES.
80	DISP	I	Auto adjustment value indication. 1: Indicated.

IC BLOCK DIAGRAM

IC, TA7291S

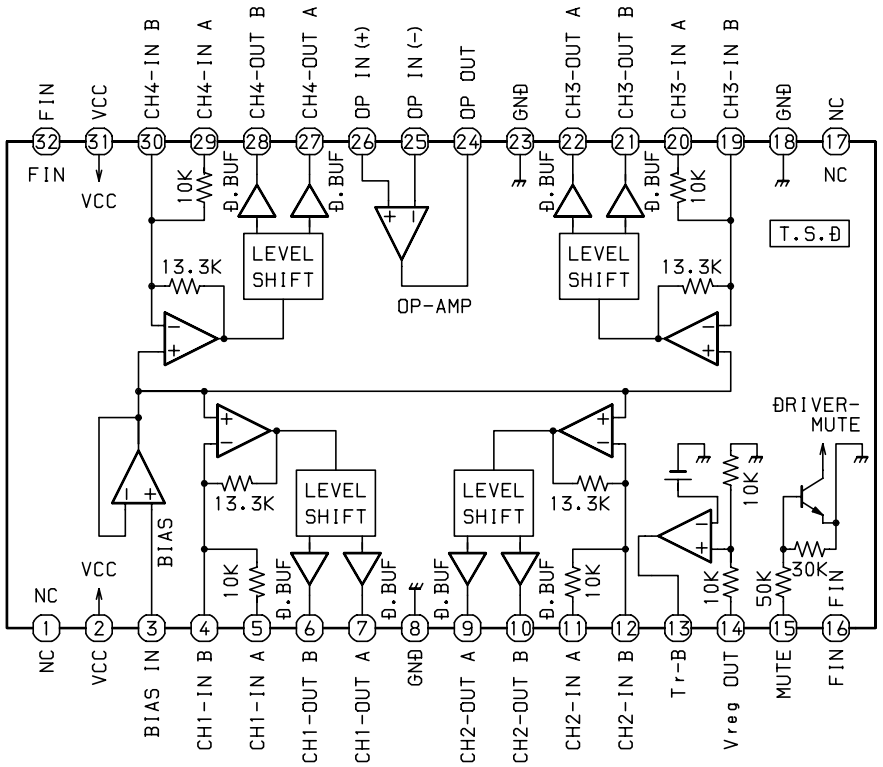


INPUT		OUTPUT		MODE
IN1	IN2	OUT1	OUT2	
0	0	∞	∞	STOP
1	0	H	L	CW/CCW
0	1	L	H	CCW/CW
1	1	L	L	BRAKE

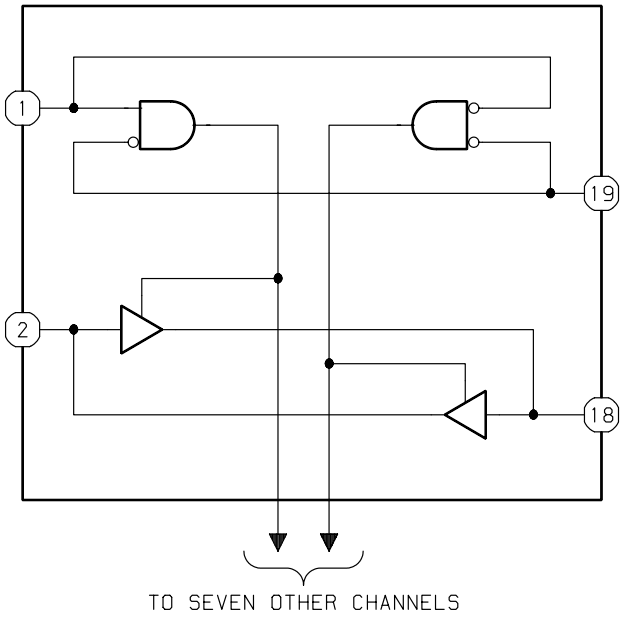
∞ : HI IMPEDANCE

NOTE : INPUT "H" ACTIVE

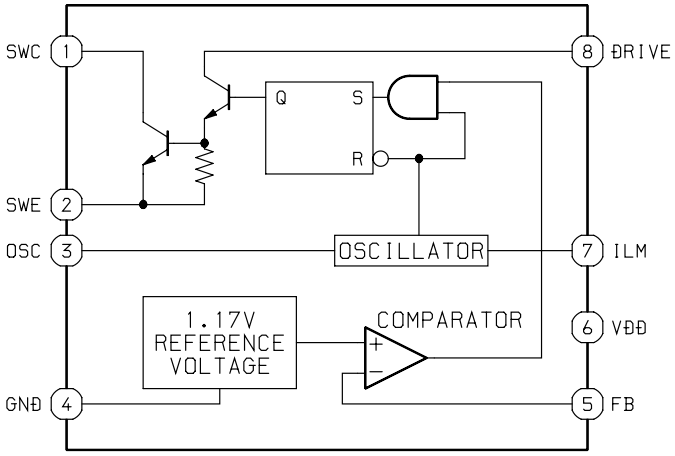
IC, BA6897



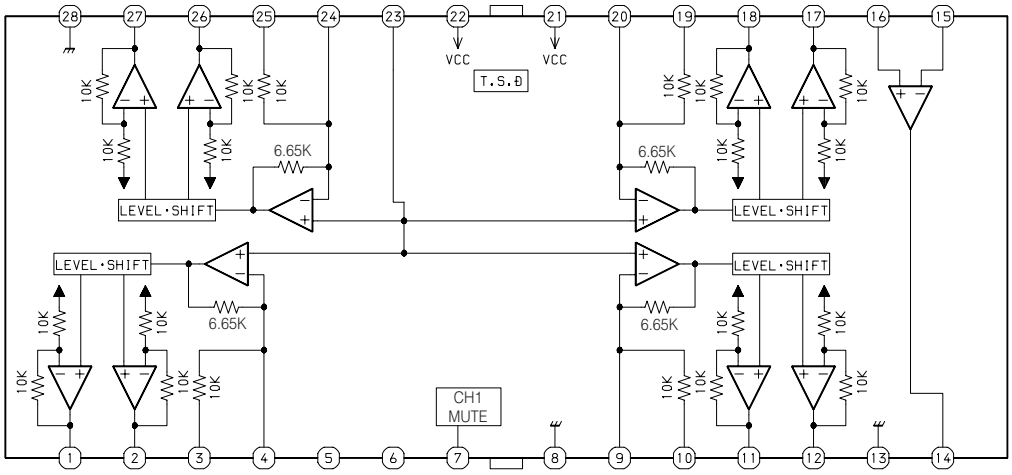
IC, SN74LS245APW



IC, M5291FP

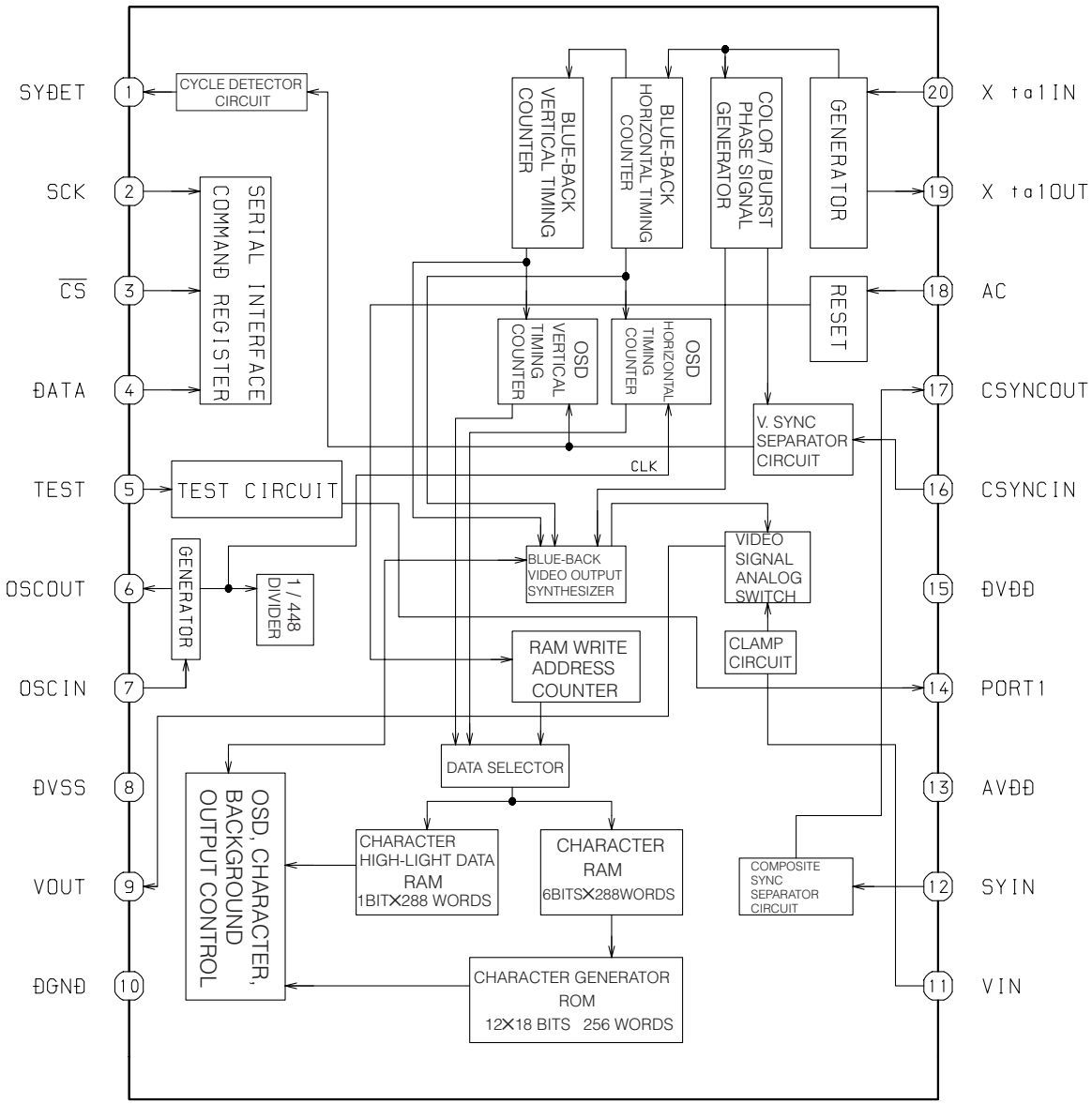


IC, BA5915



T.S.D: Thermal shut-down
Resistors are in units of Ω.

IC, BU2874AFV



TEST MODE

< How to Enter the Test Mode >

While pressing the PROGRAM key, insert the AC power cord to AC wall outlet.

< When the Machine Has Entered the Test Mode >

The system is initialized and the main power is turned on. During the test mode, the main power of the CD block is turned on always. The test mode starts with the [Sled mode].

< Types of Test Mode >

[Sled mode]

All displays of the FL tubes light. The optical pickup can be moved by pressing [⟨⟨] or [⟩⟩] key.

Pressing the [□] key establishes the [Focus mode].
Pressing the [▷] key establishes the [Play mode].

Pressing the [⟨⟨] key moves the sled to outer circumference.
Pressing the [⟩⟩] key moves the sled to inner circumference.
Pressing OPEN/CLOSE key opens or closes the tray.

[Focus mode]

Lighting of all displays of the FL tubes are turned off and returns to normal display. The focus search is performed in the focus mode regardless whether disc is inserted or not, or focus OK or NG. (Numbers of times of focus search is unlimited. Auto sequence is not used.)
Focus servo is not locked in even the focus is obtained.

Pressing the [▷] key establishes the [Play mode].
Pressing the [⟨⟨] key decreases the track number to -1.
Pressing the [⟩⟩] key increases the track number to +1.
Pressing OPEN/CLOSE key opens or closes the tray.
The machine enters the [Sled mode].

[Play mode]

Lighting of all displays of the FL tubes are turned off and returns to normal display. The focus search (numbers of search is unlimited) is performed. When focus comes to in-focus, the focus servo is locked in and the machines enters the normal play mode.
During [Play mode], GFS and sound skipping are not monitored.
When focus becomes out-of-focus, another attempt is made to search for focus.
The tracking servo and the sled servo can be turned on and off by pressing the [▷] key.

Pressing the [□] key establishes the [Sled mode].
The [||] display can be turned on and off by pressing the [▷] key .

While the [||] display is turned off:
CLV-A Tracking servo: on
Sled servo: on
While the [||] display is turned on:
CLV-A Tracking servo: off
Sled servo: off

Pressing the [⟨⟨] key decreases the track number to -1.
Pressing the [⟩⟩] key increases the track number to +1.
Pressing OPEN/CLOSE key opens or closes the tray.
The machine enters the [Sled mode].

< How to Exit the Test Mode >

Remove the AC power cord from power outlet, or turn off the system power.

The focus bias, tracking balance and the tracking gain adjustment values can be displayed, modified, set and released in the Play mode only of the following Test mode.
When the PRGM button is pressed during Play, the adjustment value of the focus bias is displayed. After that, you can enter the followings:

- FOCUS - BIAS

  [Display]: Pressing the RANDOM key during disc play, the focus bias setting value is displayed.
  [Adjustment]: Every pressing of the ⏮ key decrements the adjustment value by 1 step.
  Every pressing of the ⏭ key increments the adjustment value by 1 step.
  [Set]: The adjustment value is set by pressing the PLAY key after adjustment. Playback a disc after setting.
  [Release]: The set value can be released by pressing the STOP key.

- TRACKING - BALANCE

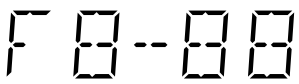
  [Display]: Pressing the REPEAT key during disc play, the tracking balance setting value is displayed.
  [Adjustment]: The same procedure as in the FOCUS - BIAS.
  [Set]: The same procedure as in the FOCUS - BIAS.
  [Release]: The same procedure as in the FOCUS - BIAS.

- TRACKING - GAIN

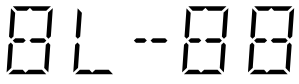
  [Display]: Pressing the DISPLAY key during disc play, the tracking balance setting value is displayed.
  [Adjustment]: The same procedure as in the FOCUS - BIAS.
  [Set]: The same procedure as in the FOCUS - BIAS.
  [Release]: The same procedure as in the FOCUS - BIAS.

Display method

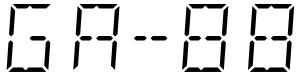
- FOCUS - BIAS



- TRACKING - BALANCE



- TRACKING - GAIN



1. How to Activate CD Test Mode
   Insert the AC plug while pressing the function CD button.
   FL display tubes will show the “start mode” display (repeating the indications “TEST” and “00 00 00” alternately), and the test mode will be activated.

2. How to Cancel CD Test Mode
   Either one of the following operations will cancel the CD test mode.
   - Press the function button. (except CD function button)
   - Press the power switch button.
   - Disconnect the AC plug

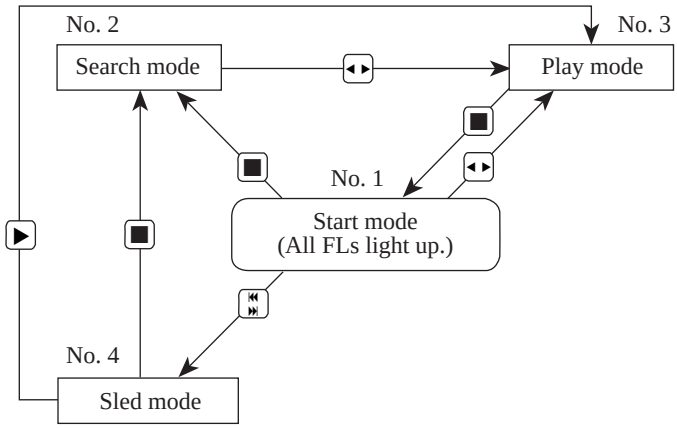
3. Description of the CD Test Mode Functions
   When test mode is activated, the following mode functions from No. 1 to No. 4 can be used by pressing the operation keys.

   [Values of Focus Balance, Tracking Balance and Tracking Gain]
   The displayed contents show the actual value after flashing three times.

Mode/No.	Operation	FL display	Operation	Contents
Start mode No.1	Activation	Start mode display	• Test mode is activated. • CD block power is ON.	• Automatic adjustment value
Search mode No.2	■ key	“ ”	• Laser diode turns always ON. • Continual focus search (The pickup lens repeats the full-swing up-down motion.) * Avoid continual searches that last for more than 10 minutes. * NOTE 1	• APC circuit check • Laser current measurement (Laser current control. Across a resistor connected between emitter and GND.) FOCUS SERVO • Check focus search waveform • Check focus error waveform (FOK/FZC are not monitored in the search mode)
Play mode No.3	◄ ► key	Normal display	• Normal playback	FOCUS SERVO/TRACKING SERVO CLV SERVO/SLED SERVO Check DRF
Sled mode No.4	⏮ key ⏭	Start mode display	• Pickup moves to the outermost track • Pickup moves to the innermost track * NOTE 2 (During playback, machine operates normally.)	SLED SERVO Check SLED mechanism operation

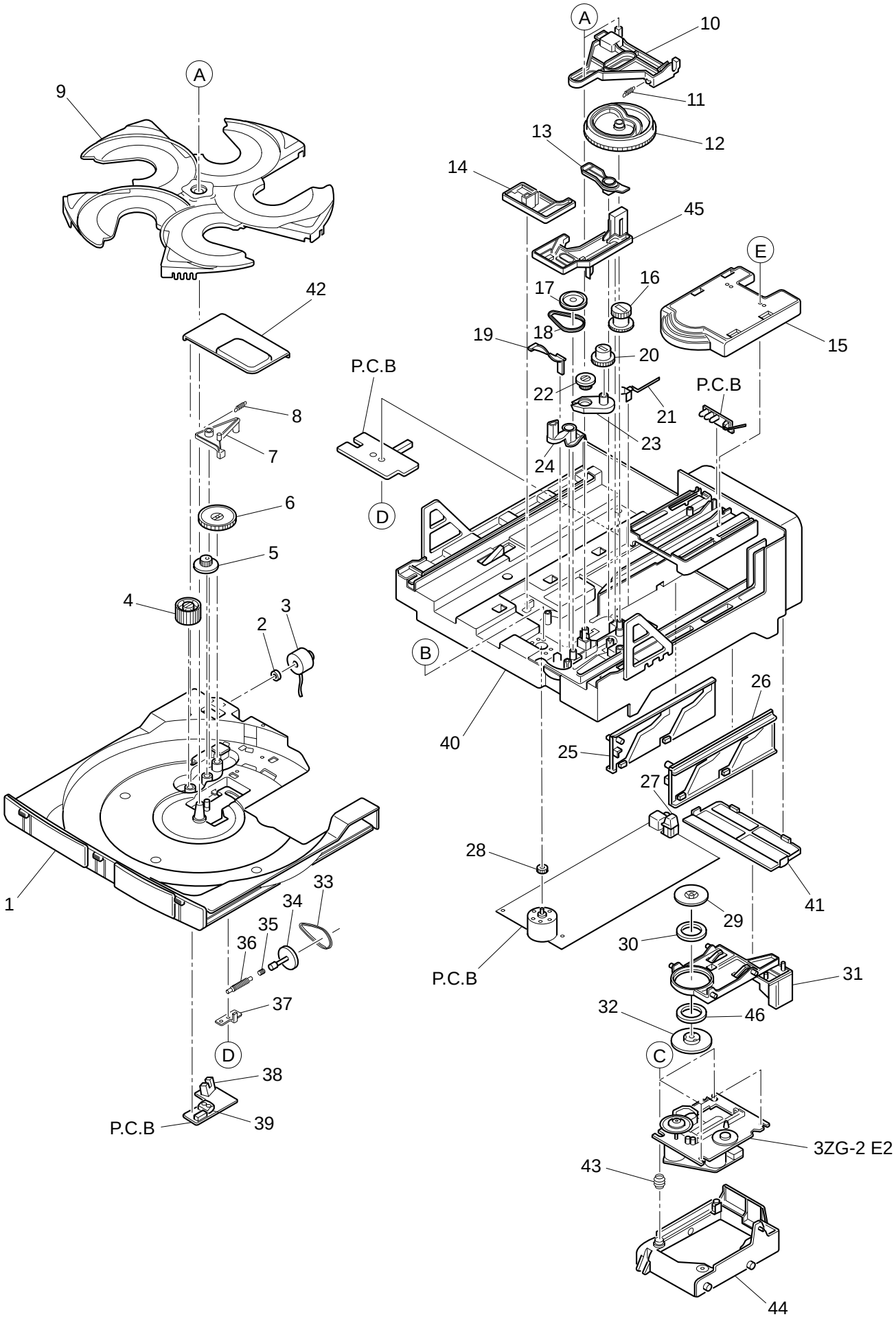
* NOTE 1: There are cases when the tracking servo cannot be locked owing to the protection circuit being operated when heat builds up in the driver IC if the focus search is operated continually for more than 10 minutes. In these cases the power supply should be switched off for 10 minutes until heat has been reduced and then re-started.
* NOTE 2: When pressing the ⏮ or ⏭ keys, take care to avoid damage to the gears. Because the sled motor is activated when the ⏮ or ⏭ keys are pressed, even when the pick-up is at the outermost or innermost track.
* NOTE 3: The machine cannot enter the traverse mode even though the PAUSE button is pressed during PLAY. It enters the normal PAUSE state.

4. Operation Outline
   The operation of each mode is carried out in the direction of the arrows from the start mode as indicated in the following illustration.



If the DISC DIRECT PLAY button is pressed, the machine performs the same operation as the PLAY button is pressed as shown. If the tray is opened by pressing OPEN/CLOSE button during Play mode or Traverse mode, the machine returns to the Start mode.

MECHANICAL EXPLODED VIEW 1/1



MECHANICAL PARTS LIST 1/1

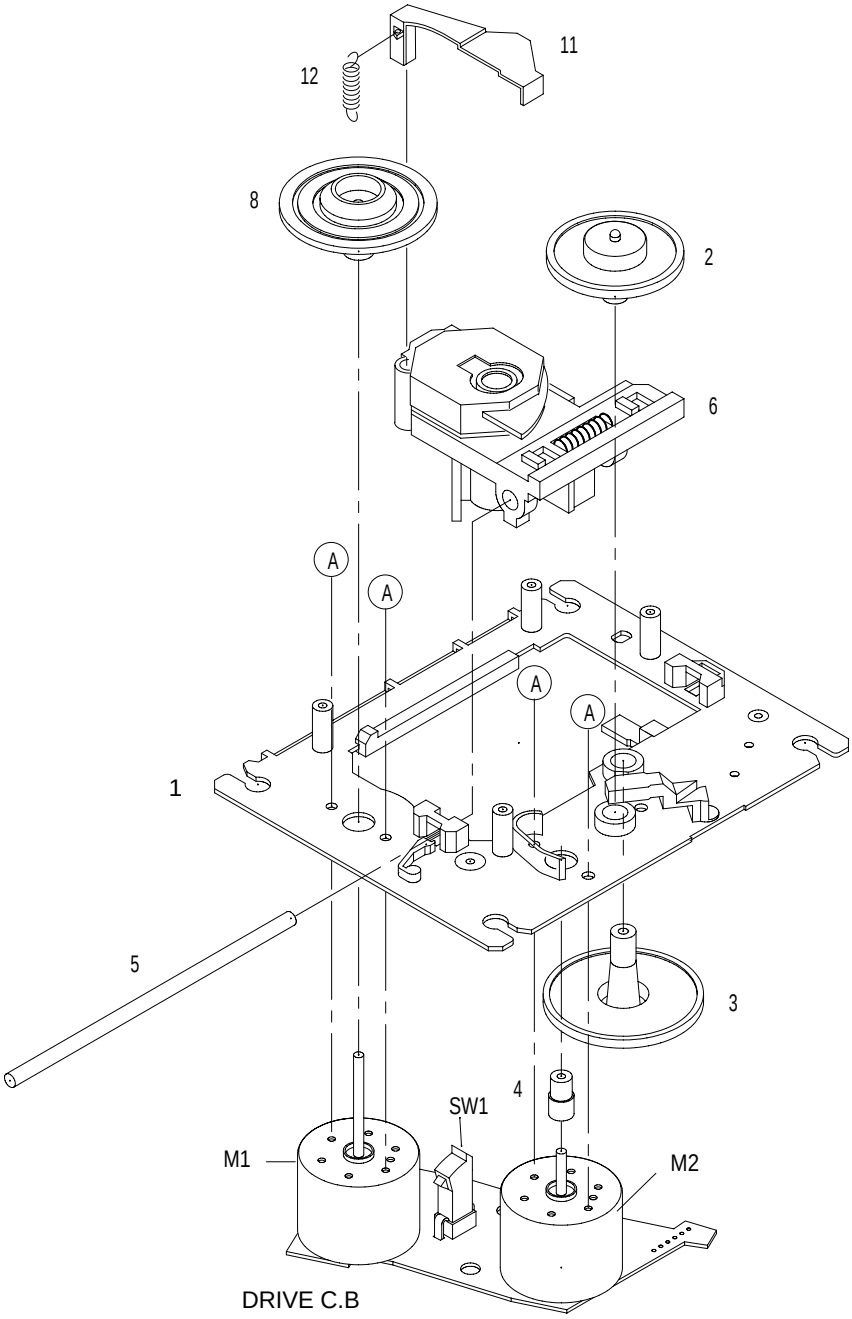
DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	86-ZG1-001-310		TRAY,5CD
2	84-ZG1-267-010		PULLEY,LOAD MO 8
3	87-A90-036-010		MOT ASSY,RF-300CA-11
4	86-ZG1-228-110		GEAR,TT-B
5	86-ZG1-227-110		GEAR,TT-A
6	86-ZG1-223-110		GEAR,WORM-WHEEL TT
7	86-ZG1-224-110		LEVER,TT(*)
8	86-ZG1-226-010		SPR-E,LEVER TT
9	86-ZG1-002-210		TURN TABLE,5CD
10	86-ZG1-211-210		JOINT,CAM
11	86-ZG1-216-010		SPR-E,JT
12	86-ZG1-203-210		GEAR,MAIN CAM
13	86-ZG1-213-110		LEVER,LOAD
14	86-ZG1-214-110		LEVER,PROTECT
15	86-ZG1-004-010		REFLECTOR,CD
16	86-ZG1-205-110		GEAR,TRAY
17	84-ZG1-207-010		PULLEY,RELAY
18	84-ZG1-209-010		BELT,SQ1.8-117.7
19	86-ZG1-217-010		LEVER,SW
20	86-ZG1-206-110		GEAR,RELAY B
21	86-ZG1-220-110		SPR-P,LOCK
22	86-ZG1-204-110		GEAR,RELAY A
23	86-ZG1-218-110		PLATE,GEAR
24	86-ZG1-208-010		LEVER,TRAY
25	86-ZG1-209-110		SLIDER,CAM L(*)
26	86-ZG1-210-110		SLIDER,CAM R(*)
27	84-ZG1-244-310		CABI,OPTICAL
28	84-ZG2-228-010		PULLEY,MOT
29	83-ZG3-211-010		PLATE,DISC<YVOS1NDM,VOS1NDSM>
29	86-ZG1-242-010		PLATE,DISC BLK <EXCEPT YVOS1NDM,VOS1NDSM>
30	83-ZG3-602-010		RING,MAG<YVOS1NDM,VOS1NDSM>
30	84-ZG1-300-010		MAGNET,CLAMPER 4P <EXCEPT YVOS1NDM,VOS1NDSM>
31	86-ZG1-215-010		HLDR,CHUCK
32	86-ZG1-238-010		HLDR,MAGNET 6ZG N
33	86-ZG1-225-010		BELT,SQ1.2-32.9
34	86-ZG1-221-010		PULLEY,TT
35	86-ZG1-231-010		SPR-C,WORM
36	84-ZG1-256-010		GEAR,WORM N2
37	86-ZG1-232-010		SPR-P,WORM
38	86-ZG1-229-010		HLDR,SENSOR
39	86-ZG1-230-010		HLDR,DISC SENSOR
40	86-ZG1-201-210		CHAS,MECHA
41	86-ZG1-005-110		COVER,CHAS
42	86-ZG1-003-110		COVER,TRAY
43	80-CD3-214-010		CUSH CD A
44	86-ZG1-202-210		HLDR,MECHA
45	86-ZG1-212-410		SLIDER,LOAD
46	86-ZG1-239-110		PLATE,DISC
A	87-078-148-010		VFT2+3-12(F10) BLK
B	87-251-072-410		U+2.6-5
C	81-ZG1-254-010		S-SCREW,MECH HLDR
D	87-067-579-010		TAPPING SCREW, BVT2+3-8
E	87-067-703-010		TAPPING SCREW, BVT2+3-10

COLOR NAME TABLE

Basic color symbol	Color	Basic color symbol	Color	Basic color symbol	Color
B	Black	C	Cream	D	Orange
G	Green	H	Gray	L	Blue
LT	Transparent Blue	N	Gold	P	Pink
R	Red	S	Silver	ST	Titan Silver
T	Brown	V	Violet	W	White
WT	Transparent White	Y	Yellow	YT	Transparent Yellow
LM	Metallic Blue	LL	Light Blue	GT	Transparent Green
LD	Dark Blue	DT	Transparent Orange		

CD MECHANISM EXPLODED VIEW 1/1 (3ZG-2 E2)



CD MECHANISM PARTS LIST 1/1 (3ZG-2 E2)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	83-ZG2-243-110		CHAS ASSY,SHT
2	83-ZG2-235-010		GEAR,A3
3	83-ZG2-205-210		GEAR,B
4	83-ZG2-236-010		GEAR MOTOR 3
5	83-ZG2-240-010		SHAFT,SLIDE 3
6	87-A90-836-010		PICKUP,KSS-213F
8	83-ZG2-233-010		TURN TABLE,A5
11	83-ZG2-245-110		LEVER,SHUTTER
12	83-ZG2-250-010		SPR-E,SHT 2
A	87-261-032-210		SCREW V+2-3

REFERENCE NAME LIST

ELECTRICAL SECTION

DESCRIPTION	REFERENCE NAME
ANT	ANTENNAS
C-	CHIP
C-CAP	CAP, CHIP
C-CAP TN	CAP, CHIP TANTALUM
C-COIL	COIL, CHIP
C-DI	DIODE, CHIP
C-DIODE	DIODE, CHIP
C-FET	FET, CHIP
C-FOTR	FILTER, CHIP
C-JACK	JACK, CHIP
C-LED	LED, CHIP
C-RES	RES, CHIP
C-SFR	SFR, CHIP
C-SLIDE SW	SLIDE SWITCH, CHIP
C-SW	SWITCH, CHIP
C-TR	TRANSISTOR, CHIP
C-VR	VOLUME, CHIP
C-ZENER	ZENER, CHIP
CAP, CER	CAP, CERA-SOL
CAP, E	CAP, ELECT
CAP, M/F	CAP, FILM
CAP, TC	CAP, CERA-SOL
CAP, TC-U	CAP, CERA-SOL SS
CAP, TN	CAP, TANTALUM
CERA FIL	FILTER, CERAMIC
CF	FILTER, CERAMIC
DL	DELAY LINE
E/CAP	CAP, ELECT
FILT	FILTER
FLTR	FILTER
FUSE RES	RES, FUSE
MOT	MOTOR
P-DIODE	PHOTO DIODE
P-SNSR	PHOTO SENSER
P-TR	PHOTO TRANSISTOR
POLY VARI	VARIABLE CAPACITOR
PPCAP	CAP, PP
PT	POWER TRANSFORMER
PTR, RES	PTR, MELF
RC	REMOTE CONTROLLER
RES NF	RES, NON-FLAMMABLE
RESO	RESONATOR
SHLD	SHIELD
SOL	SOLENOID
SPKR	SPEAKER
SW, LVR	SWITCH, LEVER
SW, RTRY	SWITCH, ROTARY
SW, SL	SWITCH, SLIDE
TC CAP	CAP, CERA-SOL
THMS	THERMISTOR
TR	TRANSISTOR
TRIMMER	CAP, TRIMMER
TUN-CAP	VARIABLE CAPACITOR
VIB, CER	RESONATOR, CERAMIC
VIB, XTAL	RESONATOR, CRYSTAL
VR	VOLUME
ZENER	DIODE, ZENER

MECHANICAL SECTION

DESCRIPTION	REFERENCE NAME
ADHESHIVE	SHEET ADHESHIVE
AZ	AZIMUTH
BAR-ANT	BAR-ANTENNA
BAT	BATTERY
BATT	BATTERY
BRG	BEARING
BTN	BUTTON
CAB	CABINET
CASS	CASSETTE
CHAS	CHASSIS
CLR	COLLAR
CONT	CONTROL
CRSR	CURSOR
CU	CUSHION
CUSH	CUSHION
DIR	DIRECTION
DUBB	DUBBING
FL	FRONT LOADING
FLY-WHL	FLYWHEEL
FR	FRONT
FUN	FUNCTION
G-CU	G-CUSHION
HDL	HANDOL
HIMERON	CLOTH
HINGE, BAT	HINGE, BATTERY
HLDR	HOLDER
HT-SINK	HEAT SINK
IB	INSTRUCTION BOOKLET
IDLE	IDLER
IND, L-R	INDICATOR, L-R
KEY, CONT	KEY, CONTROL
KEY, PRGM	KEY, PROGRAM
KNOB, SL	KNOB, SLIDE
LBL	LABEL
LID, BATT	LID, BATTERY
LID, CASS	LID, CASSETTE
LVR	LEVER
P-SP	P-SPRING
PANEL, CONT	PANEL, CONTROL
PANEL, FR	PANEL, FRONT
PRGM	PROGRAM
PULLY, LOAD MO	PULLY, LOAD MOTOR
RBN	RIBBON
S-	SPECIAL
SEG	SEGMENT
SH	SHEET
SHLD-SH	SHIELD-SHEET
SL	SLIDE
SP	SPRING
SP-SCREW	SPECIAL-SCREW
SPACER, BAT	SPACER, BATTERY
SPR	SPRING
SPR-P	P-SPRING
SPR-PC-PUSH	P-SPRING, C-PUSH
T-SP	T-SPRING
TERM	TERMINAL
TRIG	TRIGGER
TUN	TUNING
VOL	VOLUME
W	WASHER
WHL	WHEEL
WORM-WHL	WORM-WHEEL

アイワ株式会社 〒110-8710 東京都台東区池之端1-2-11 ☎03(3827)3111 (代表)
AIWA CO.,LTD. 2–11, IKENOHATA 1–CHOME, TAITO-KU, TOKYO 110-8710, JAPAN TEL:03 (3827) 3111

931261
Printed in Singapore